AMPEX
AUDIO-VIDEO
SYSTEMS DIVISION

VPR-2

CHARACTER GENERATOR ACCESSORY

OPERATION AND MAINTENANCE

CATALOG NO. 1809447-02
CHANGED: JANUARY 1981

Catalog No. 1809447-02
Issued: April 1980
Changed: January 1981

VPR-2
CHARACTER GENERATOR ACCESSORY

OPERATION AND MAINTENANCE

AMPEX CORPORATION
AUDIO-VIDEO SYSTEMS DIVISION

Prepared by

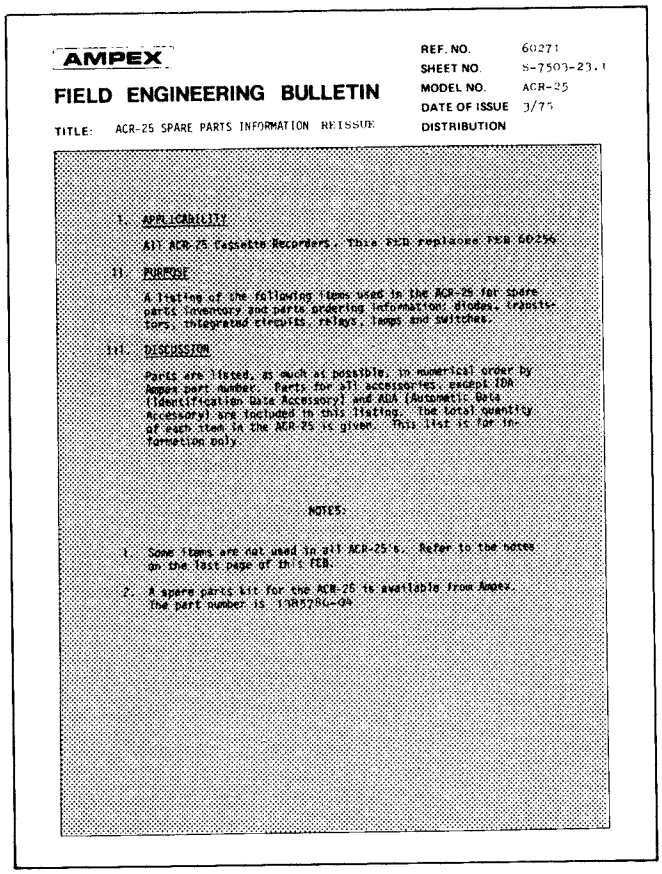
AVSD Technical Publications
Ampex Corporation
401 Broadway
Redwood City, CA 94063

Catalog No. 1809447-02
Issued: April 1980
Changed: January 1981

PRINTED IN USA

FOR ADDITIONAL TECHNICAL INFORMATION

FIELD ENGINEERING BULLETIN SERVICE



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FIELD ENGINEERING BULLETIN

REF. NO. 60271
SHEET NO. S-7503-23.1
MODEL NO. ACR-25
DATE OF ISSUE 3/75
DISTRIBUTION

TITLE: ACR-25 SPARE PARTS INFORMATION REISSUE

I. APPLICABILITY

All ACR-25 Cassette Recorders. This FEB replaces FEB 60256

II. PURPOSE

A listing of the following items used in the ACR-25 for spare parts inventory and parts ordering information: diodes, transistors, integrated circuits, relays, lamps and switches.

III. DISCUSSION

Parts are listed, as much as possible, in numerical order by Ampex part number. Parts for all accessories, except IDA (Identification Data Accessory) and ADA (Automatic Data Accessory) are included in this listing. The total quantity of each item in the ACR-25 is given. This list is for information only.

NOTES:

1. Some items are not used in all ACR-25's. Refer to the notes on the last page of this FEB.
2. A spare parts kit for the ACR-25 is available from Ampex. The part number is 13R3784-04.

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Effective: 1 September 1978

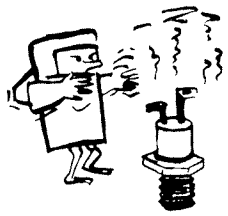
SAFETY AND FIRST AID SUGGESTIONS

Regardless of how well electrical equipment is designed, personnel can be exposed to **dangerous electrical shock** when protective covers are removed for maintenance or other activities. Therefore, it is incumbent on the user to see that all safety regulations are consistently observed and that each individual assigned to the equipment has a clear understanding of first aid related to electrical hazards.

In addition, the following safety practices must be followed:

1 Do not attempt to adjust unprotected circuit controls or to dress leads with power **on**.

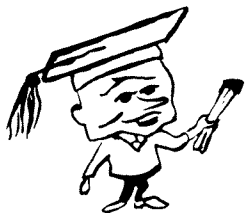
2 Do not touch heavily loaded or overheated components without precaution to avoid burns.



3 Do not assume that all danger of electrical shock is removed when power is off. Charged capacitors can retain dangerous voltages for a long time after power is removed. These capacitors should be discharged through a suitable resistor before any circuit points are touched.

4 Always avoid placing parts of the body in series between ground and circuit points.

5 Remember that some semiconductor cases and solid-state circuits carry high voltages.



6 Don't take chances. Be fully trained. Ampex equipment should be operated and maintained only by fully qualified personnel.

If someone seems unable to free himself while receiving an electrical shock, **turn power off** before attempting to render aid. A muscular spasm or unconsciousness can make a victim unable to free himself from the electrical power.

WARNING

DO NOT
TOUCH VICTIM OR HIS CLOTHING BEFORE
POWER IS REMOVED OR YOU MAY ALSO
BECOME A SHOCK VICTIM

If power cannot be removed immediately, **very carefully** loop a length of dry nonconducting material (such as rope, insulating material, or clothing) around the victim and pull him free of the power. Carefully avoid touching him or his clothing until free of power. Immediately start the appropriate first aid procedures.

GOOD PRACTICES

In maintaining the equipment covered in this manual, please keep in mind the following standard good practices:

1. When connecting any instrument (oscilloscope, waveform monitor, etc.) to a high-frequency output, use the appropriate termination resistor at the input of the instrument, unless the instrument is terminated internally.

2. When inserting or removing printed wiring assemblies (PWAs), cable connectors, or fuses, always turn off power to the affected portion of the equipment. After power is removed, allow sufficient time for the power supplies to bleed down before reinserting PWAs.

3. When troubleshooting, remember that FETs and other metal-oxide-semiconductor (MOS) devices may appear defective because of leakage between traces or component leads on the printed wiring board. Clean the printed wiring board and recheck the MOS device before assuming it is defective.

4. When replacing MOS devices, follow standard practices to avoid damage caused by static charges and soldering.

5. When removing components from PWAs (particularly ICs), use care to avoid damaging PWA traces.

WARNING

This equipment generates, uses, and can radiate radio frequency energy and if not installed and used in accordance with the instruction manual, may cause interference to radio communications. As temporarily permitted by regulation it has not been tested for compliance with the limits for Class A computing devices pursuant to Subpart J of Part 15 of FCC Rules, which are designed to provide reasonable protection against such interference. Operation of this equipment in a residential area is likely to cause interference in which case the user at his own expense will be required to take whatever measures may be required to correct the interference.

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SECTION 1

GENERAL INFORMATION

1-1. PURPOSE AND SCOPE OF MANUAL

This manual provides information on installation, operation, theory of operation, and maintenance of the VPR-2 Character Generator PWA, Ampex Part No. 1400073, which is an accessory to the VPR-2 Video Production Recorder.

1-2. CAPABILITIES OF THE CHARACTER GENERATOR

The Character Generator PWA receives all of its inputs (except video) from or through the Time-Code Reader/Generator (TCR/G) PWA. Therefore, it can be used only in VPR-2 recorders in which a TCR/G PWA is installed. The character generator provides a monitor screen readout of the output of the TCR/G display selector. The display provided by the character generator is an eight-digit readout of the tape program time in hours, minutes, seconds, and frames. In addition to providing display of the two tape timers, the Character Generator PWA can also provide monitor display of time from the time code on the tape audio 3 track during playback. It can also provide monitor display of time from the time-code generator during code generation. The eight-digit monitor time display tracks the LED time readout on the VPR-2 control panel. The character generator can also display hexadecimal data from the TCR/G on the monitor when the TCR/G is in user mode.

The monitor time display identifies the source of time data with a two- or three-character prefix.

The character generator produces a monochrome display of the tape time in any of four character/background formats and in any of four character sizes. The display can be either black or white characters shown against a contrasting background field called a window; or the characters can be shown against a contrasting border that frames the contours of the individual character. The character size options are such that the smallest display is about one-fourth the screen width and the largest display occupies almost a full screen width. A horizontal control and a vertical control permit the display to be positioned anywhere on the screen.

1-3. PHYSICAL DESCRIPTION

The VPR-2 character generator accessory consists of one printed wiring assembly (PWA). The PWA is installed in slot number 7 of the VPR-2 electronics assembly which is located immediately below the VPR-2 control panel. Placarding for the control devices on the Character Generator PWA is shown on the inside of the door of the electronics assembly. See Figure 1-1.

1-4. RELATED PUBLICATIONS

Publications containing information relevant to the VPR-2 Video Production Recorder and the Character Generator PWA are as follows:

- VPR-2 Time-Code Reader/Generator Accessory Operation and Maintenance, Ampex Catalog No. 1809449
- VPR-2 Video Production Recorder Installation and Operation, Ampex Catalog No. 1809379

1-5. FUNCTIONAL DESCRIPTION

The Character Generator PWA produces an on-screen numerical readout of tape time data supplied

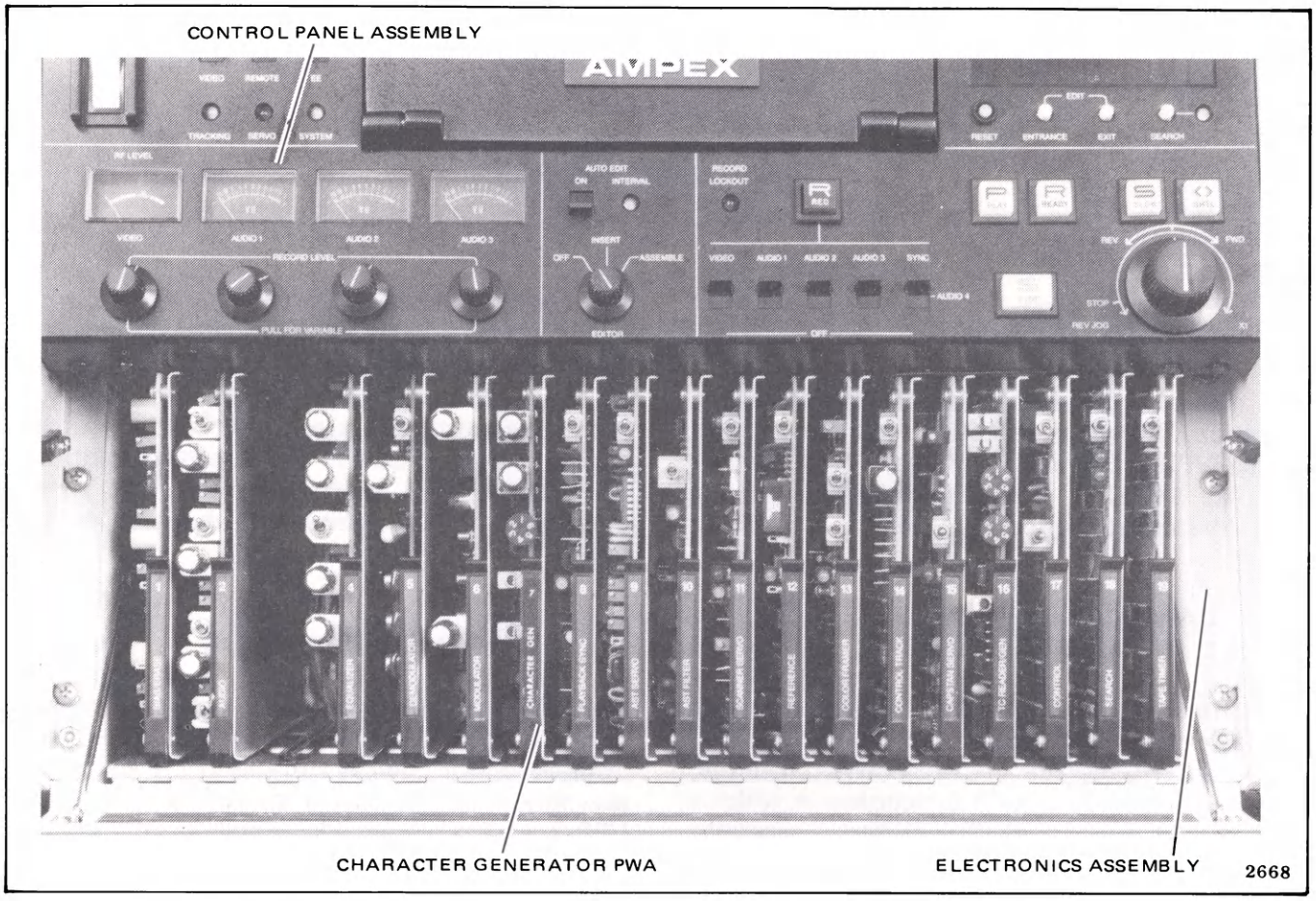


Figure 1-1. VPR-2 Character Generator PWA Installed in VPR-2 Recorder

by tape timer 1, tape timer 2, or the time-code reader/generator. This is done by multiplexing black and white levels with composite video. The black and white levels form the elements of the displayed characters and their borders. Each character fits into a 7-row-by-7-column-element matrix. The black and white elements for each character and its border are stored in a read-only memory (ROM) in the form of eight binary words 12 bits long. Each of the eight binary words represents the elements of one row or horizontal slice of a character. The black and white elements are inserted into the composite video by the composite video-black-white multiplex logic. See Figure 1-2. A new character element is produced each time a bit is shifted out of the character/border horizontal slice shift register. This shift register is parallel loaded with a horizontal character slice from the character storage ROM just prior to the time the character slice is to be displayed. The character slice is addressed by both the partial address formed by the data to be displayed and the partial address formed by the horizontal and vertical position counters. Display data from one of the four sources is presented to the data inputs of a RAM. Clock pulses from the TCR/G PWA are shaped to form write enable pulses for the RAM. The data enters the PWA in a serial stream of eight binary coded decimals (BCD), two BCD's for each of the hours, minutes, seconds, and frame numbers. The data in the storage RAM is updated once during the beginning of each frame. At the appropriate time in a raster scan, the horizontal/vertical position counter addresses the location in the RAM containing the number to be displayed. The addressed number is then used to address the location in the character storage ROM that contains the black/white element information required to display the number.

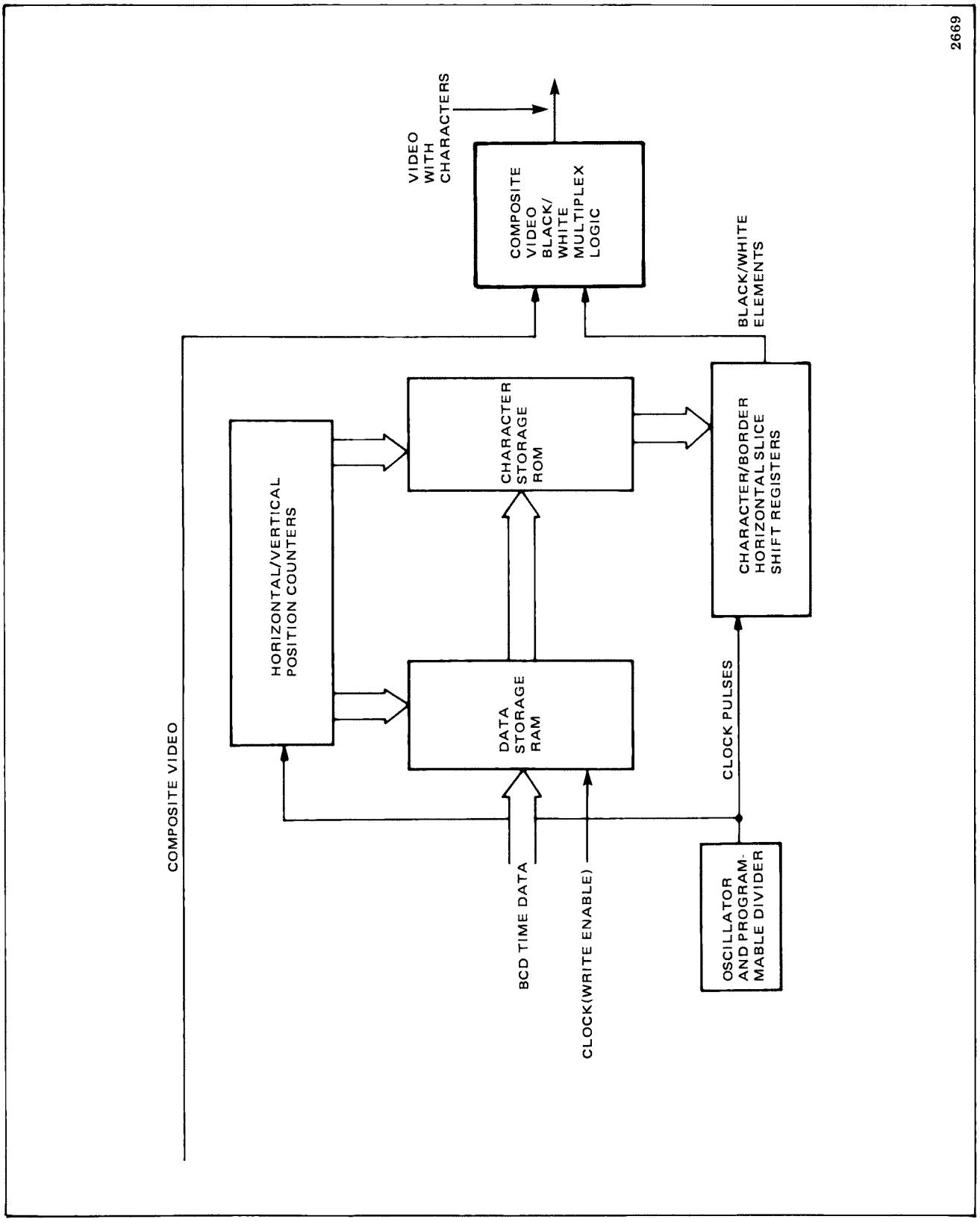


Figure 1-2. Character Generator PWA Simplified Block Diagram

SECTION 2
INSTALLATION

2-1. INTRODUCTION

Video Bypass PWA, Ampex Part No. 1401073, is installed in slot 7 of the electronics assembly of VPR-2 recorders which do not include a Character Generator PWA. The Video Bypass PWA contains three coaxial conductors which simply provide paths across the card for three video signals: VIDEO 1, VIDEO 2, and VIDEO MON. No circuitry is involved. The Character Generator PWA, which is to be installed in slot 7, includes the three video bypass conductors. The video bypass conductors are independent of the character generator circuitry.

2-2. INSTALLATION

NOTE

Before installing the Character Generator PWA, check the serial number of the VPR-2 recorder. If the serial number is 399 or lower, inspect the wiring between XA7 on the VPR-2 electronics assembly motherboard and connectors J16, J17, and J18 on the rear connector panel for conformance with Figure 2-1. If the wiring does not conform with Figure 2-1, the VPR-2 must be modified in accordance with Ampex Instruction No. 1809456-01 before installing the Character Generator PWA.

2-3. Parts Required

The parts required for installation of a Character Generator PWA in both console-mounted VPR-2 recorders and VPR-2 recorders not mounted in a console are contained in Ampex Kit No. 1400235.

2-4. Console Installation

Install the Character Generator PWA in the VPR-2 recorder as follows:

1. Turn off the VPR-2 main power.
2. Open the door of the electronics assembly.
3. Remove the Video Bypass PWA from slot 7 of the electronics assembly.
4. Insert the Character Generator PWA into slot 7 of the electronics assembly.
5. Interconnect the VPR-2 recorder, TBC-2 time-base corrector, and the monitor in accordance with Figure 2-1.
6. Turn on the VPR-2 main power.
7. Check out operation of the Character Generator PWA as referenced in paragraph 2-6.

2-5. Non-Console Installation

Interconnect signals between the VPR-1 electronics assembly, the TBC-2 Time-Base Corrector, and the monitor in accordance with Figure 2-2. This provides time display characters in the normal video monitoring path. The user may, however, connect the character generator in any configuration desired. Check out operation of the Character Generator PWA as referenced in paragraph 2-6.

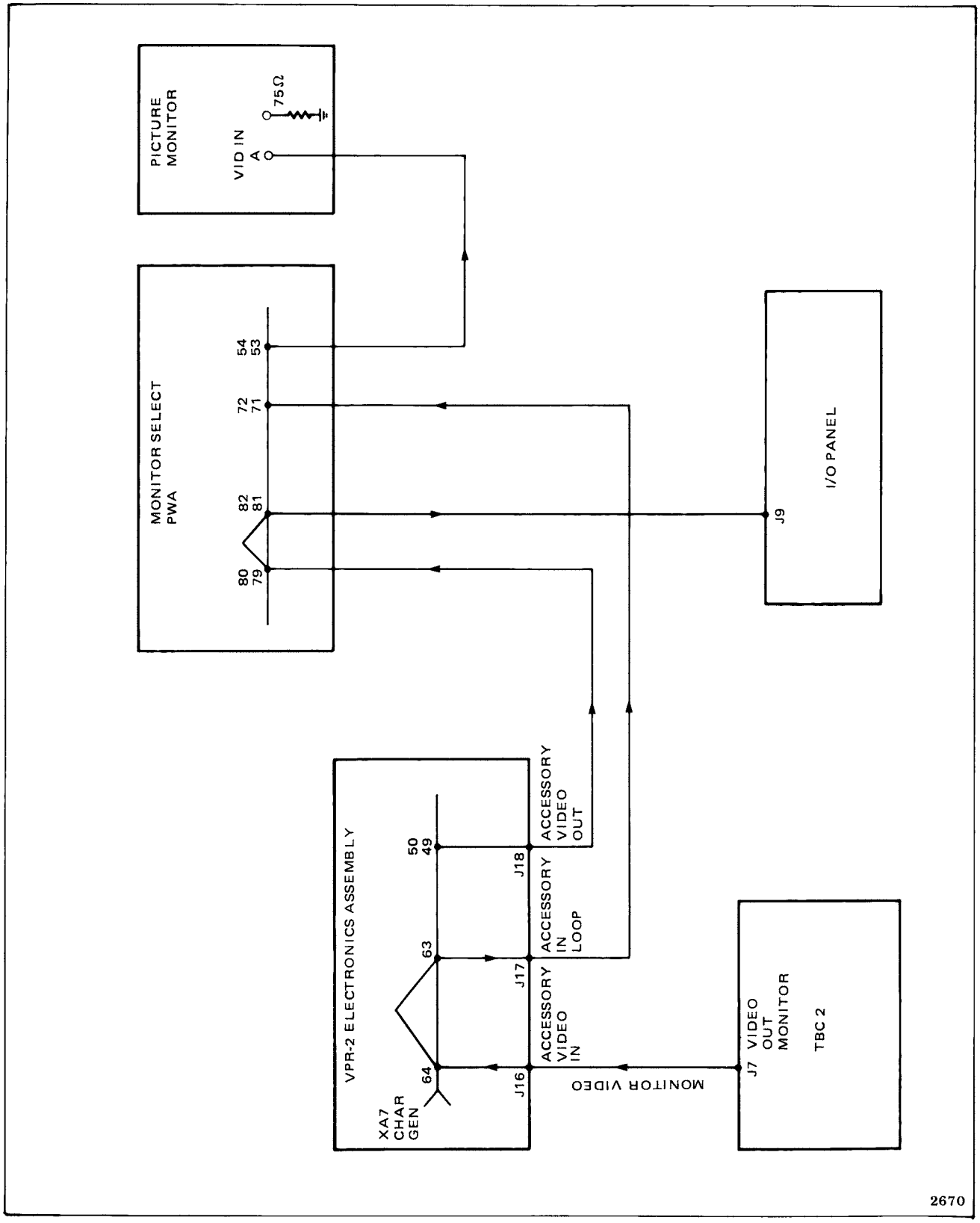


Figure 2-1. Character Generator Signal Path in VPR-2 Console and Monitor Bridge

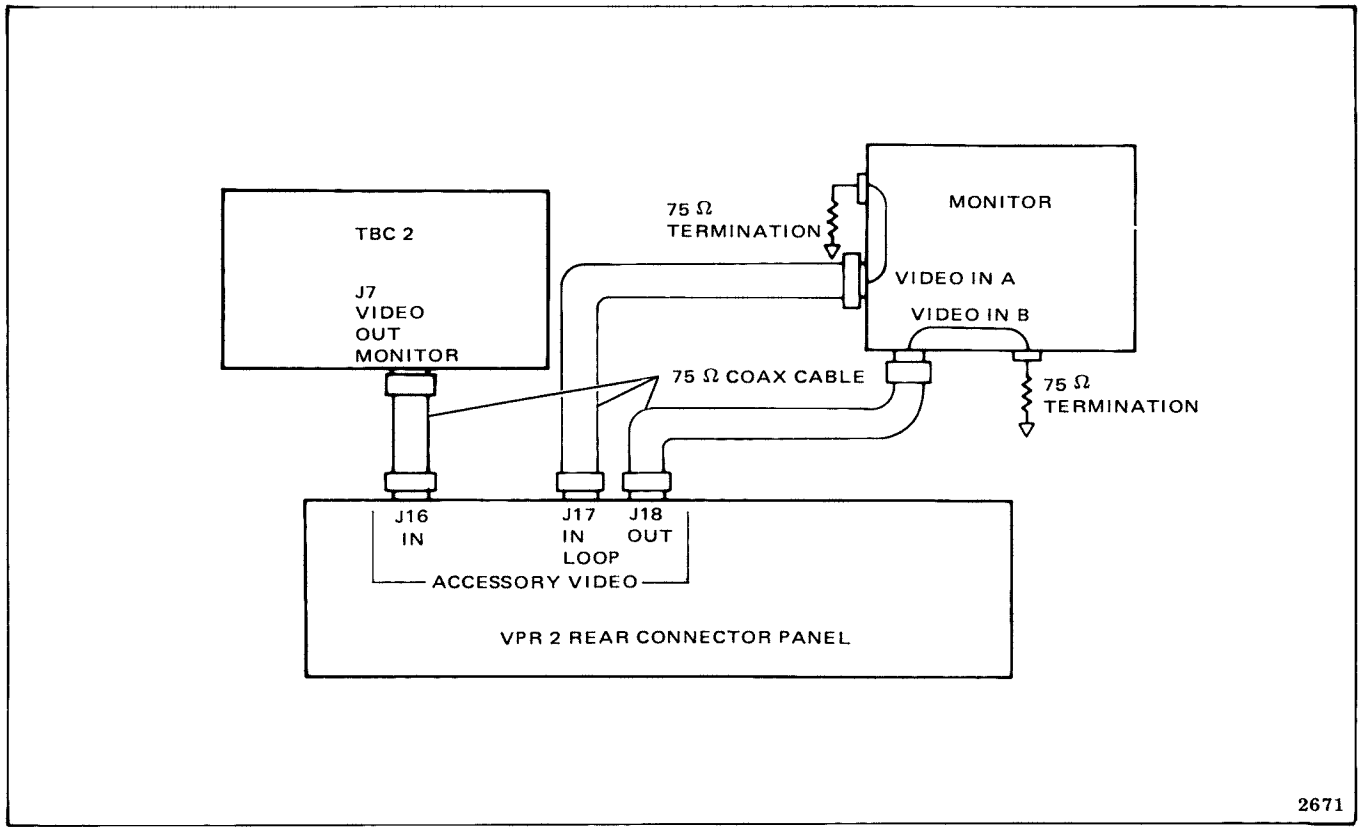


Figure 2-2. Character Generator Suggested Interconnection Diagram (Non-Console Installation)

NOTE

If the Character Generator PWA is removed from the electronics assembly for maintenance, remember to install the Video Bypass PWA in its place in slot 7. Failure to thus maintain continuity of the three video signal paths will render the VPR-2 inoperative.

2-6. CHECKOUT

Checkout of the character generator performance is accomplished by performing part of the diagnostic procedure contained in the Operation and Maintenance Manual for the VPR-2 time-code reader/generator. Step the time-code reader/generator output through every possible character in each character position, as shown in Figure 4-3. Check the monitor display of the character generator output for conformance with the LED display on the VPR-2 control panel. Check the monitor display of the character generator output with the time-code reader/generator in all modes of operation with and without tape in motion to observe all of the types of displays shown in Figure 3-1.

This checkout assumes that the time-code reader/generator is fully operational. Non-conformance with any of the above would indicate a fault within the Character Generator PWA.

SECTION 3
OPERATION

3-1. INTRODUCTION

This section of the manual explains the functions of the controls on the Character Generator PWA. The different types of monitor displays are illustrated and operating instructions for the Character Generator PWA are provided.

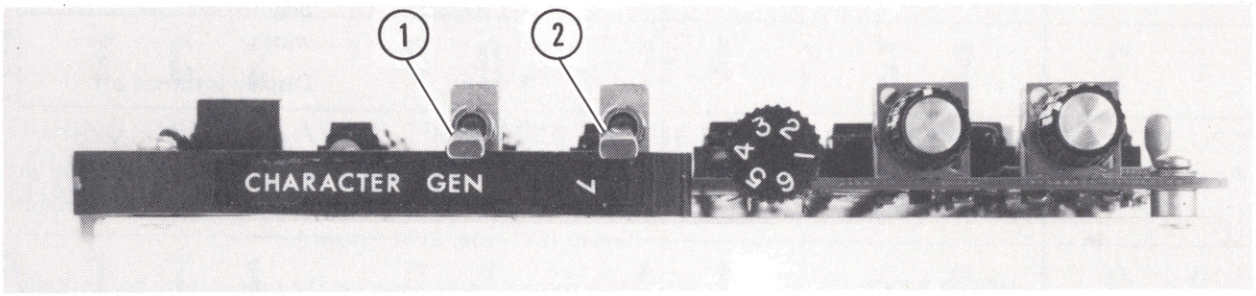
3-2. CONTROLS

Table 3-1 lists the names and functions of the controls on the front edge of the Character Generator PWA.

3-3. MODES OF OPERATION

Controls of the time display by the Character Generator PWA are listed in Table 3-1 (character size, screen position, black/white polarity, and border/window display). All inputs to the Character Generator PWA which govern character content are provided by the Time-Code Reader/Generator PWA, part no. 1400160. Figure 3-1 shows samples of the basic types of displays. Display types may also appear in combination, depending upon status provided by the Time-Code Reader/Generator PWA.

Table 3-1. Character Generator PWA Controls



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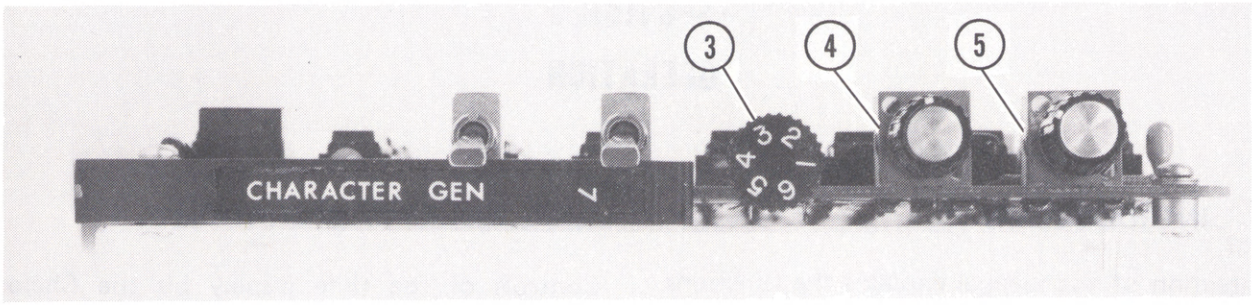
INDEX NO.	NAME	FUNCTION
1	BLACK/WHITE toggle switch	When set to WHITE, tape time is displayed in white letters on a black background. When set to BLACK, display is in black letters on a white background. Background can be a border or a window, depending on the setting of the BORD/WINDOW toggle switch.
2	BORD/WINDOW toggle switch	When set to BORD, each character of the time display is individually framed with a contrasting border; program video is visible between the frames characters. When set to WINDOW, the characters of the display are shown against a contrasting window that frames the entire time display; program video is not visible between the characters.

Table 3-1. Character Generator PWA Controls (Continued)



INDEX NO.	NAME	FUNCTION
3	CHAR SIZE rotary switch	This switch determines the size of the displayed characters as follows. POSITION — DISPLAY WIDTH 1 SMALL — Slightly more than one quarter of screen width 2 MED/SMALL — Slightly less than half of screen width 3 MED — Slightly more than half of screen width 4 LARGE — Slightly less than full screen width 5 OFF — Display is turned off 6 OFF
4	VERT POSITION potentiometer	This control permits placing the time display vertically to any location between the top and bottom of the monitor screen (CW = up, CCW = down).
5	HORIZ POSITION potentiometer	This control permits placing the time display horizontally to any position between the left and right sides of the screen. The control has no effect when the CHAR SIZE rotary switch is set to 4 LARGE (CW = right, CCW = left).

The eight-digit numerical display of hours, minutes, seconds, and frames separated by colons (or semicolons in drop frame) on the monitor screen tracks the LED indicators on the tape timer section of the VPR-2 control panel. Neither colons nor semicolons are used in the monitor display when the TCR/G is in user mode. Source and status of time data are indicated by the three-character alphanumeric prefix.

As shown in Figure 3-1A and B, prefix TT1 or TT2 indicates that the source of time data is tape timer 1 or 2, respectively. Similarly, prefix TC1 or TC2 indicates that source of time data is the Time-Code Reader/Generator PWA. If time data is being read from the tape, the black/white polarity of the prefix is uniform with the numerical display (Figure 3-1C). If the time-code generator

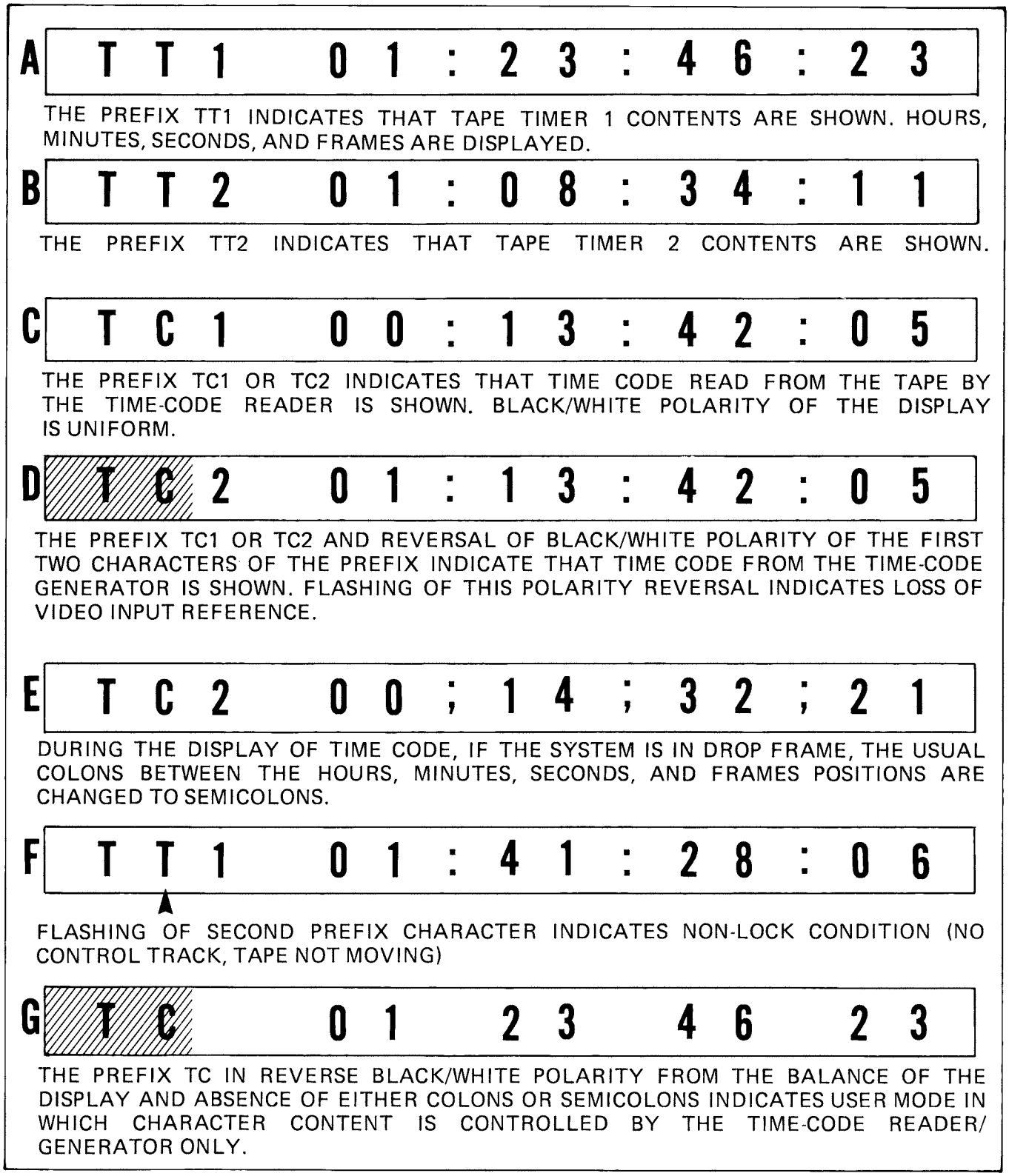


Figure 3-1. Character Generator Display Types

is providing the time data, the black/white polarity of prefix letters TC is reversed from the rest of the display (Figure 3-1D). Drop frame is indicated by the substitution of semicolons for colons (Figure 3-1E). On/off flashing of the second prefix character, T or C, indicates a non-lock condition (no control track, tape not moving), as shown in Figure 3-1F. The prefix TC (third character blanked) in reverse black/white polarity and absense of colons or semicolons indicates user mode (Figure 3-1G).

3-4. OPERATION

Operate the character generator as follows:

1. Turn on the VPR-2 main power.

2. Turn on the VPR-2 monitor.

3. Turn on the Character Generator PWA by rotating the CHAR SIZE switch from position 5 (or 6) to the desired character size setting.

4. Select mode of operation using the controls on the Time-Code Reader/Generator PWA in slot 16.

5. Start tape motion.

6. Set the BORD/WINDOW switch as required depending on the background desired.

7. Set the BLACK/WHITE switch to BLACK to display black characters on white, or to WHITE to display white characters on black.

8. Position the time display on the monitor screen by adjusting the VERT POSITION and HORIZ POSITION controls.

SECTION 4
THEORY OF OPERATION

4-1. INTRODUCTION

The Character Generator PWA produces an on-screen numerical readout of tape time data supplied by tape timer 1, tape timer 2, the time-code reader, or the time-code generator. This is done by multiplexing black and white levels with composite video. The black and white levels form the elements of the displayed characters and their borders. Each character fits into a 7-row-by-7-column-element matrix. The black and white elements for each character and its border are stored in a read-only memory (ROM) in the form of eight binary words 12 bits long. Each of the eight binary words represents the elements of one row or horizontal slice of a character.

4-2. DISPLAY FORMAT

Figure 4-1 shows how a character is formed on the monitor screen. The letter "T" is drawn as it is shown on the raster when the small character size is chosen. The character is shown white with a black border. The character is made up of individual elements. The letter "T", including the border, is 7 elements high by 7 elements wide. A black element is formed when the video is switched off and a black level reference voltage is switched on in its place. A white element is formed when the video is switched off and a white level reference voltage is switched on in its place.

Figure 4-2 shows the design of each of the characters (with their borders) that can be displayed by the Character Generator PWA.

The upper portion of Figure 4-3 shows a typical tape time display. There are 16 positions in the display which are numbered 0 to 15. The chart shown under the typical display (Figure 4-3) lists all of the possible characters that can be displayed in each of the 16 positions of the display. Positions 3 and 15 are always blank. Position 0 displays a "T" only. Position 1 can display a "T", "C", or be blank. Position 2 can display a 1 or 2 or be blank. Position pairs 4 and 5, 7 and 8, 10 and 11, 13 and 14 are the hours, minutes, seconds, and frame position pairs, respectively. The hours position pair displays up to 99 hours. The minutes and seconds position pairs display up to 59 minutes and seconds. The chart also indicates that additional numbers and letters can be displayed in these positions as a function of the Time-Code Reader/Generator PWA. Positions 6, 9, and 12 can display either a colon or a semicolon, or they can be blank. Position 15 is always blank.

4-3. THEORY

The theory of operation of the Character Generator PWA is described with Figure 4-4, Character Generator PWA Functional Block Diagram, used as an aid. In many areas of the theory, where greater detail is given, schematic diagram 1400075, (shown in Section 6 of this manual) is required as a reference.

4-4. Border Data and Character Data Shift Registers, Black-White-Composite Video Switches

Just prior to the scan of a character position on the raster, the border data shift register A25 and the character data shift register A4 are parallel-loaded with data (from ROM A18) that is required to produce the elements of a horizontal slice of the character to be displayed. See Figure 4-5. The data in these registers is shifted into the video-black-white level control circuit A41, A40, A44 in time with the clock pulses produced by the frequency

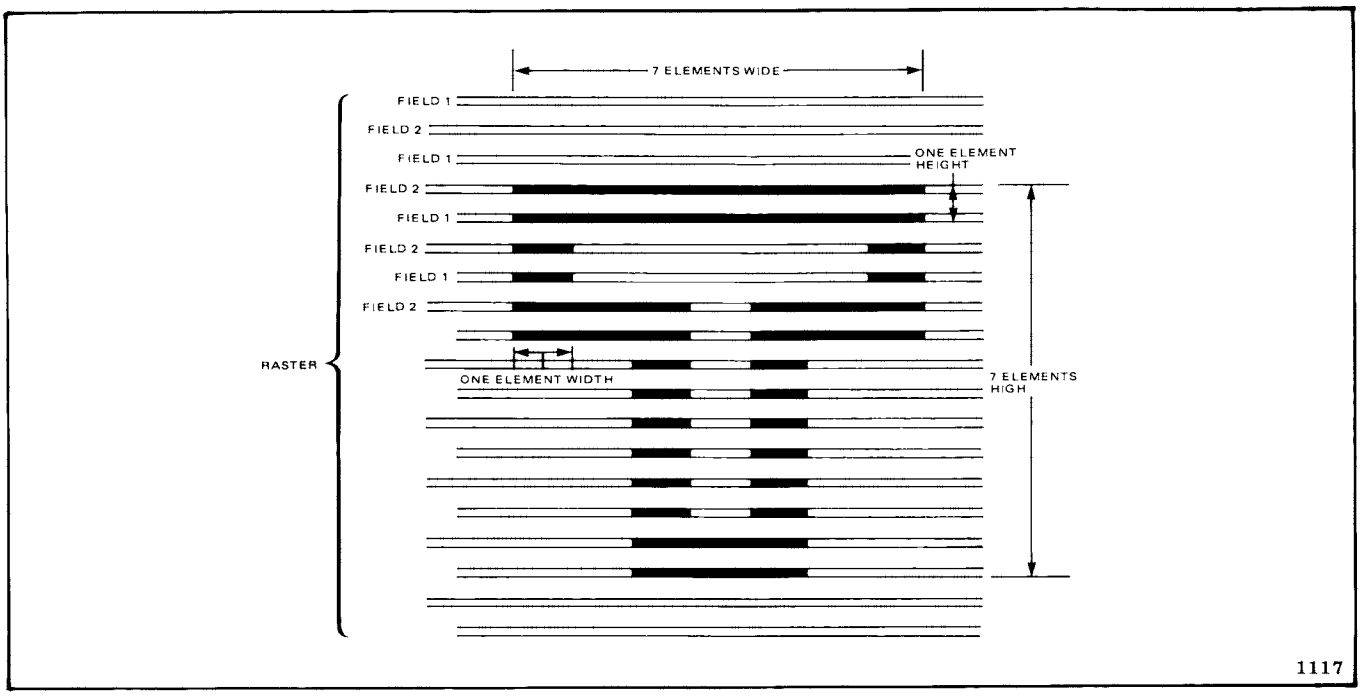


Figure 4-1. The Letter "T" as Displayed on the Monitor (Small Size, White Character with a Black Border, NTSC Raster)

divider circuit A3. The period of the clock pulse determines the size of the horizontal element. At each clock pulse, the video-black-white level control circuit examines the two parallel bits shifted out of the registers and turns on either the video switch, the black level switch, or the white level switch. Only one switch can be on at a time. When the video switch is on, composite program video from X2 video amplifier A51 is applied to the video-out line on PWA pin 29 through line driver A46. When the black switch is on, the black level reference voltage produced by the black level reference voltage circuit R43, R44 is applied to the line driver. When the white level switch is on, the white level reference voltage produced by the white level reference voltage circuit R45, R48, is applied to the line driver. A horizontal slice of a character is formed by this method of alternately switching in the appropriate reference voltage or video as the character position is scanned. Figure 4-5 shows how the vertical element No. 4 of the character "T" is formed. In this figure, two horizontal lines form a vertical element. This is representative of the smallest characters that the Character Generator PWA produces in 525-line standards. In 625-line standards, there are four horizontal lines per vertical element.

SECAM video input is indicated when the source identification line at PWA pin 35 goes high. In this case, the identification input, buffered by A34-13, is applied to switch A45-12. The amplified composite video signal is applied to the bandpass filter composed of L2, L4, C34, Q3, Q4, and Q5. The filter output, which is the center phase of the SECAM signal, is applied to switch A45-10. Thus, with SECAM video, the output of switch A45-11 mixes with the black and white reference signals on the video-out line. If the source identification line at PWA pin 35 is low, indicating NTSC/PAL video, switch A45-12 is not turned on, and the output of the SECAM bandpass filter is inhibited.

4-5. ROM A18 Data Format

ROM A18 is a 1024 word by 12-bit read-only memory in which the character and border information for each character is permanently stored. The ROM is arranged into 128 blocks of memory locations. Each block contains eight sequential

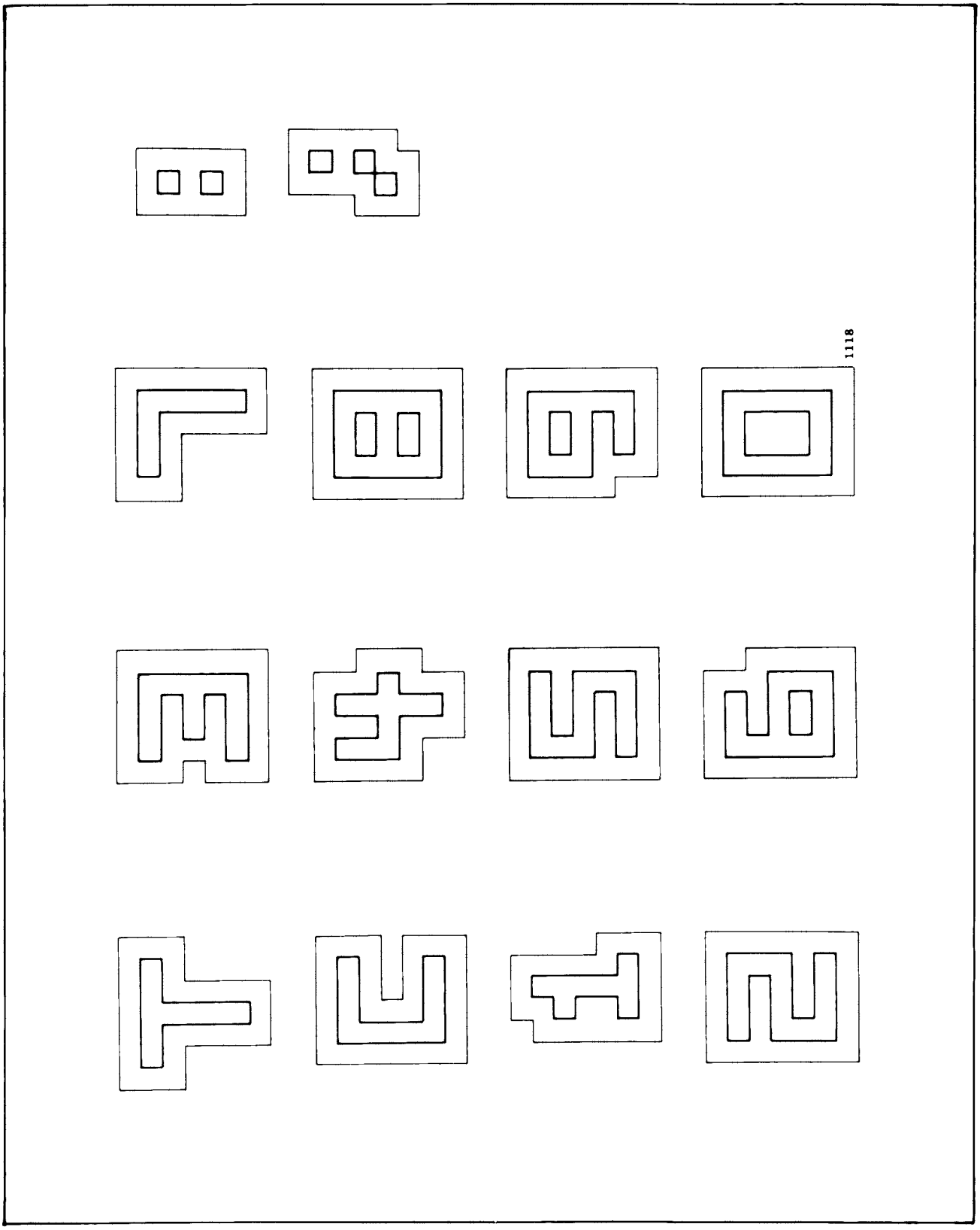


Figure 4-2. Character and Border Style

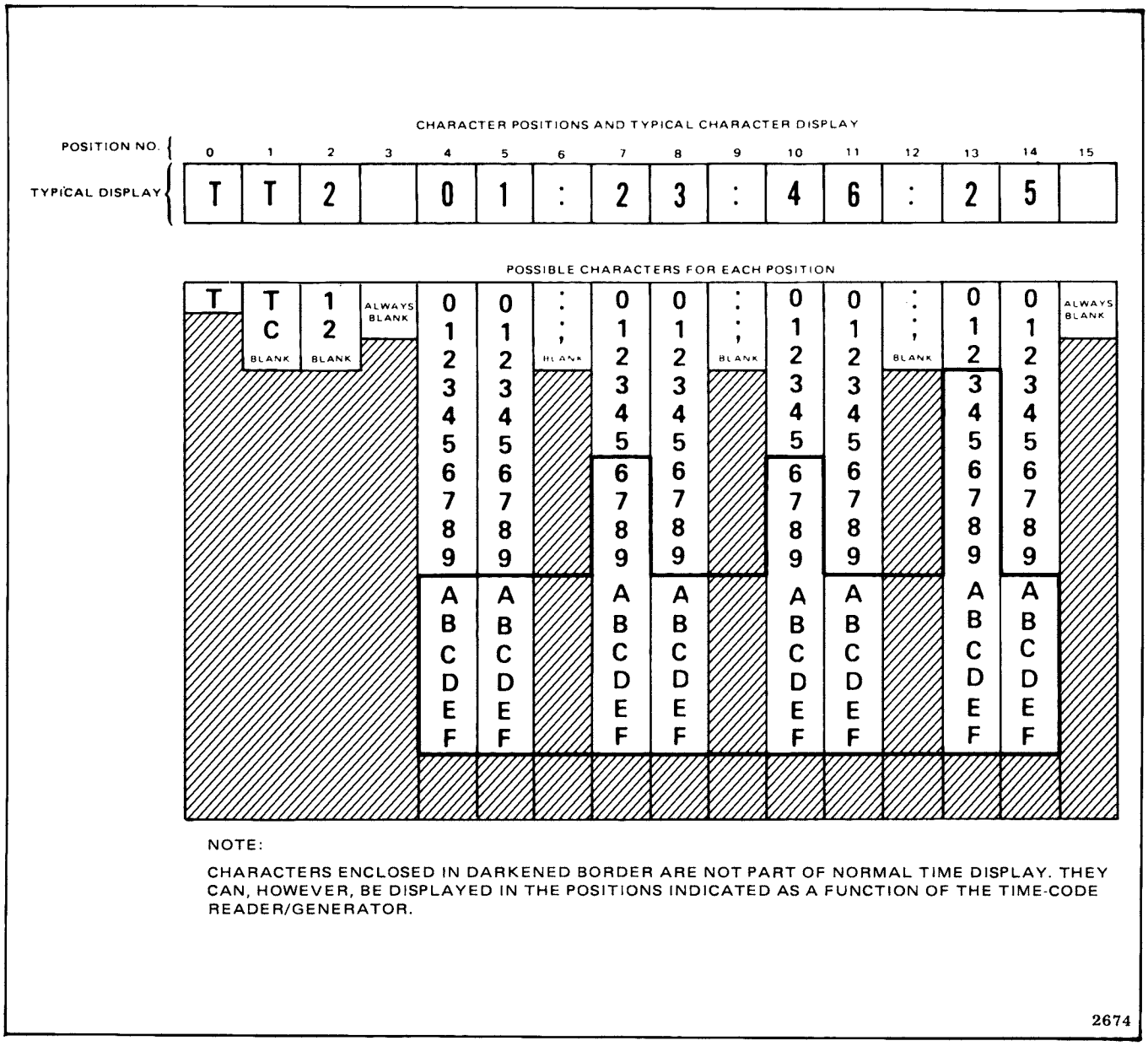


Figure 4-3. Character Positions, Typical Character Display and Possible Characters in Each Position

12-bit locations and stores all the data necessary to define a particular character and its border. Each memory location stores a 12-bit binary word. Each word defines the elements of one horizontal slice of a character and its border. Data stored in the ROM is loaded into registers A4 and A25. See Figure 4-6. The data content of the ROM is shown in Table 4-1. In this table the 128 blocks of memory have been arranged in 8 rows of 16 columns. At the intersection of each row and column are found eight sequential memory locations that contain a character. The address and content of each memory location is written as two hexadecimal numbers. The encoded character is shown next to each block of data. When the hexadecimal numbers defining the bit pattern stored in the eight memory locations of a block are converted to binary numbers, the character stored

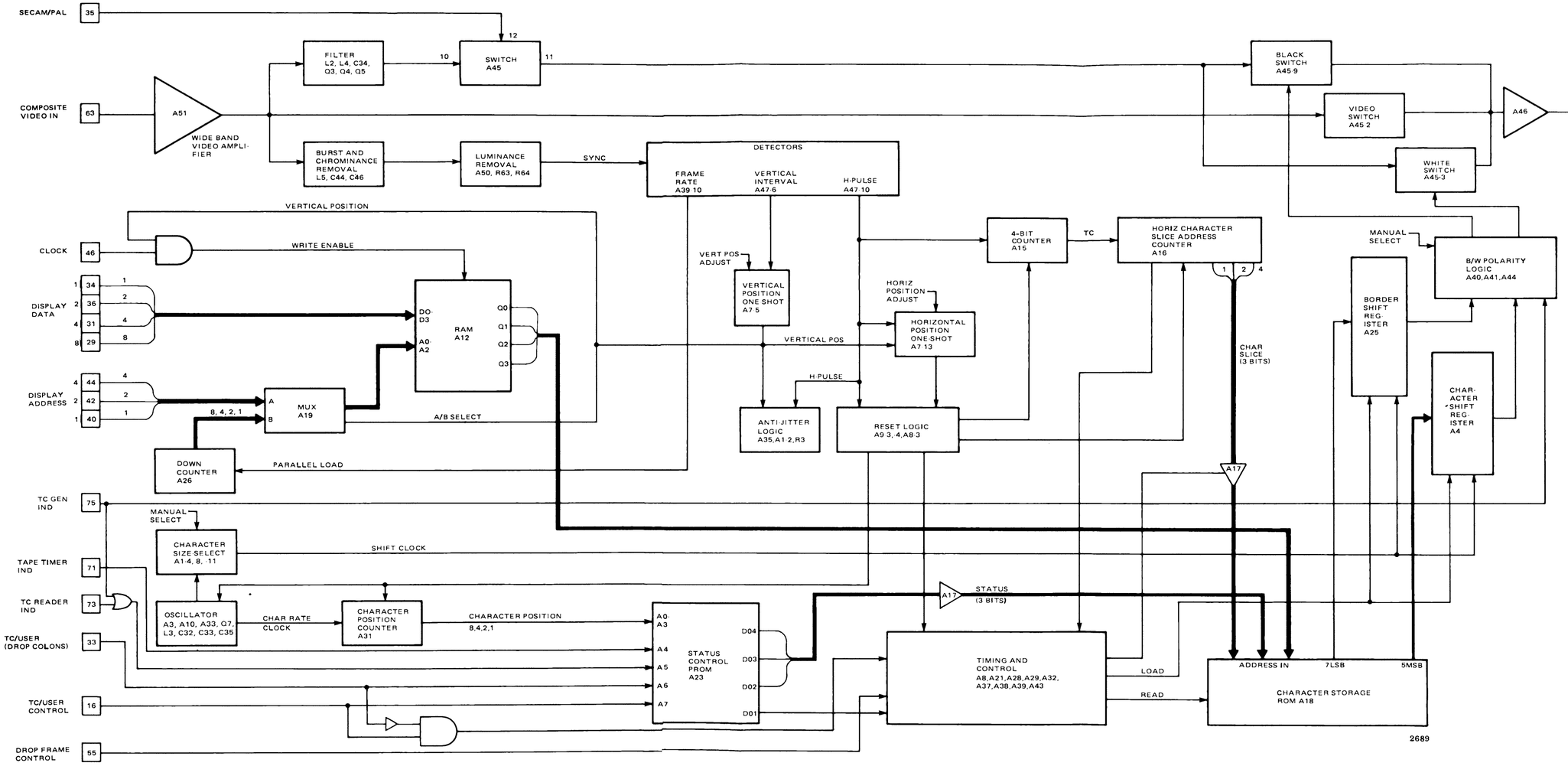


Figure 4-4.
Character Generator PWA
Functional Block Diagram

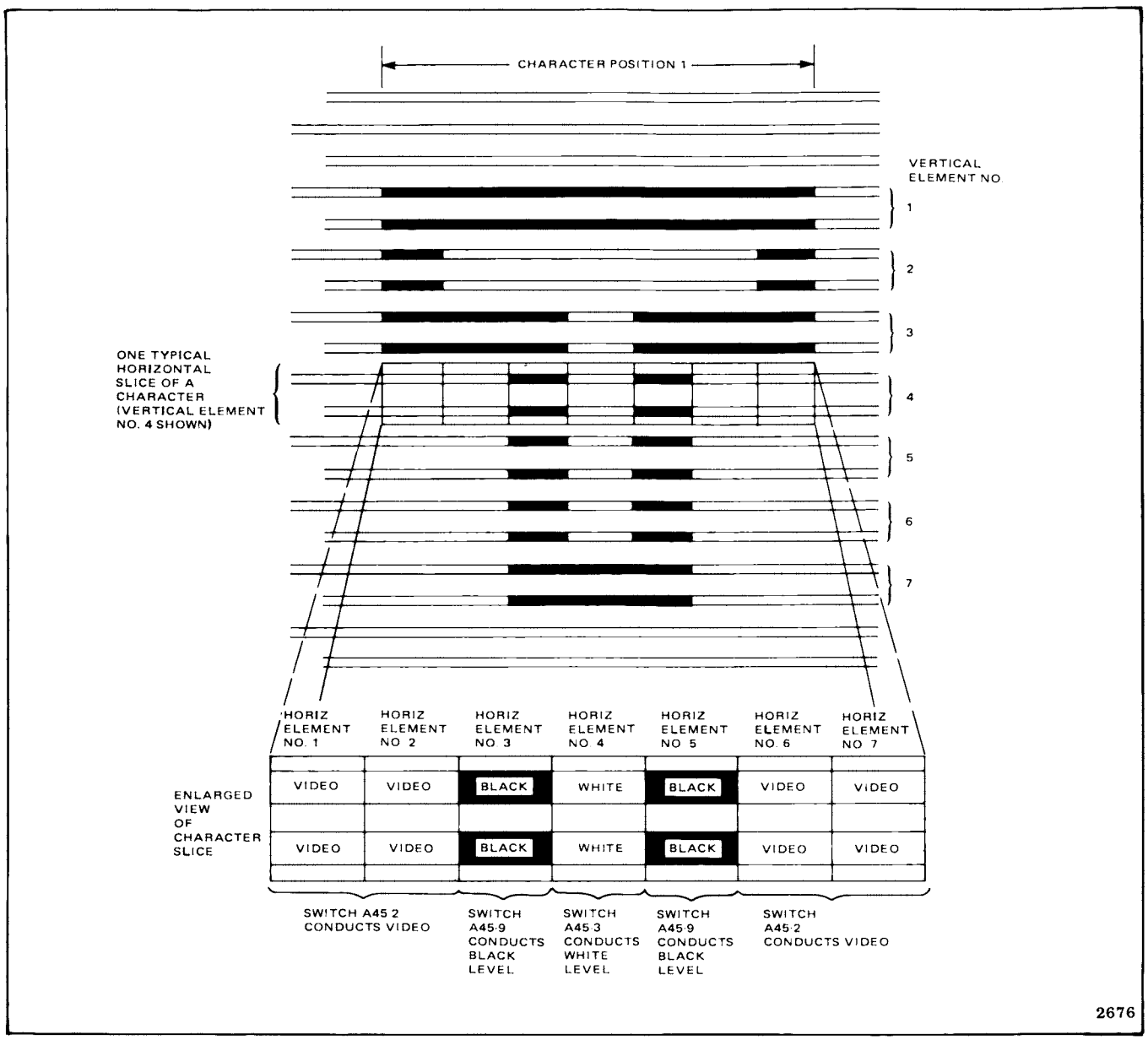


Figure 4-5. Typical Horizontal Slice of a Character — White with Black Border, NTSC Raster

in the block can be seen. Referring to Table 4-1, the character stored at the intersection of row 1 and column 5 is the letter "T". This is made apparent in Figure 4-6, where the hexadecimal data in the eight memory locations has been converted in binary numbers. The binary numbers show the state of each memory cell of the 12-cell memory location. The 1's in the array of the eight binary numbers form the image of two "T's" side-by-side and have been outlined in Figure 4-6. The "T" formed of the leftmost bits of the eight memory locations forms the character information of the "T". These bits are used to form the elements of the character itself. The "T" formed by the right-most 7 bits of the eight memory locations comprises the border information of the "T". These 7 bits are used to generate the elements that surround the character. Figure 4-6 also illustrates

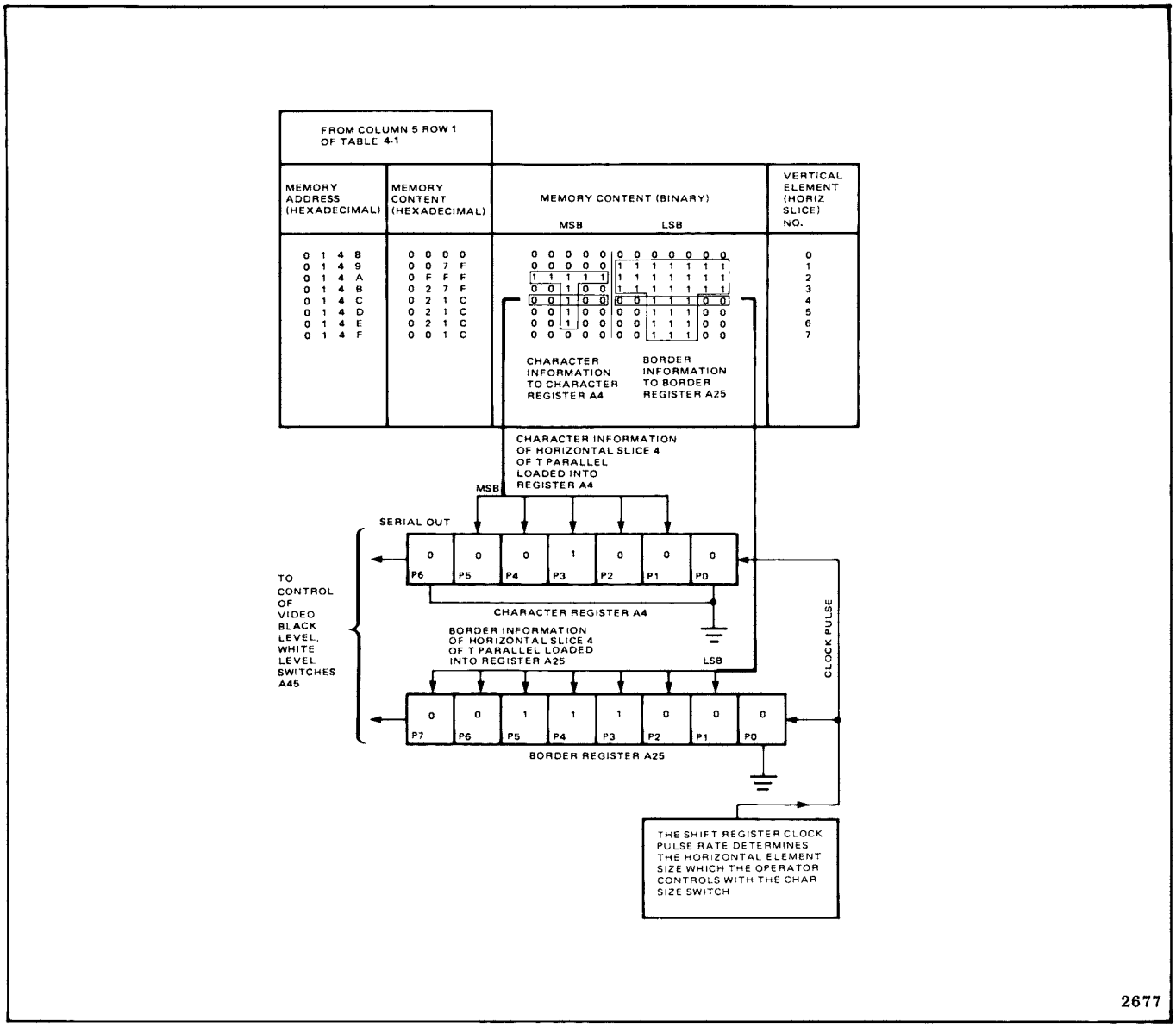


Figure 4-6. ROM A18 Storage Format of a Character

how the binary number residing in a memory location is used to form a horizontal slice of a character. Data handling for the production of horizontal slice number 4 is shown as an example. The 5 bits of character information of the slice are shown parallel-loaded in serial shift register A4 and seven bits of border information are shown simultaneously parallel-loaded in serial shift register A25. The information in both of these registers is simultaneously shifted out serially to the video control logic by a clock pulse. Whenever a "1" is shifted out of the border register A25, the video-black-white level switch control circuit A41, A40, A44, turns off the composite video at PWA output pin 29 and at the same time enables either the black level reference voltage or the white level reference voltage. When a "1" bit from the border registers turns off the composite video, the video control logic examines the bit coming out of character register A4. When the BLACK/WHITE switch

on the front of the PWA is set to WHITE (white letters on a black background), a "0" at the output of the character register causes the control logic to enable the black level voltage through switch A45 to the video output line. This forms a black element. A "1" at the character register output switches the white level voltage onto the video output line to form a white character element. When the BLACK/WHITE switch is set to BLACK, a "0" from the character register produces a white element and a "1" produces a black element.

When the BORDER/WINDOW switch is set to WINDOW, a "1" is loaded into the border shift register A25 at P7 with each clock pulse. This causes a "1" to be read out of the border shift register at each clock pulse regardless of what border information was supplied from the ROM. As before, a "1" at the output of the border shift register turns off the composite video at the output of switch A45 and enables the black level and white level switches. This has the effect of extending the border to encompass all of the element positions of the character field. This results in the characters of the display being seen against contrasting field or window.

4-6. Character Addressing

Each of the characters displayed is stored in one (or more) of the 128 blocks of memory in character storage ROM A18. A character address is formed of three distinct types of information that are combined to form the complete character address. The three types of information are the character position count, status information, and display data.

The character position count (4 lines) and status information (4 lines) are encoded in status control PROM A23 into a three-bit partial address that is applied to the address lines of character storage ROM A18. Display data (4 lines) comprises an additional four-bit partial address applied to ROM A18. These two partial addresses provide the seven bits of addressing required to locate any of the 128 characters. In addition, another type of address is required to locate each of the eight horizontal slices of character that reside in the eight memory locations that comprise a block of memory. The horizontal character slice address (3 bits) is produced by the horizontal character slice address former, A16. See Figure 4-7.

Status control PROM A23 generates a 3-bit partial address. This partial address locates groups of characters in character storage ROM A18. The eight-bit input address to PROM A23 comprises 4 bits from the character position counter A31 and 4 bits of status information derived from inputs from the time-code reader/generator (TCR/G).

The character position counter A31 produces a binary count of the 16 character positions that comprise the display. The count is advanced just before each new character position is scanned. Character position count information is relevant to character addressing since not all the character positions display the same characters (see Figure 4-3).

The 4 bits of status information are derived from the following five inputs: (1) tape timer indication at PWA pin 71; (2) time-code reader indication at pin 73; (3) time-code generator indication at pin 75; (4) time-code/user (drop colons) line at pin 33; and (5) time-code/user control line at pin 16. Of the first 3 inputs, only one can be true at a time, indicating the discrete source of the time data. These inputs are low true and cause character position 2 to be a "T" or "C". B/W polarity reversal to indicate time-code generator input is caused by the high output of AND gate A29-10 during character times 0 and 1. When the input at PWA pin 55 is low true, colons normally displayed in character positions 6, 9, and 12 are changed to semicolons. When the input at PWA pin 33 is low true, indicating TCR/G user mode, character positions 6, 9, and 12 are blanked.

Table 4-2 shows the contents of status control PROM A23. The coding chart for PROM A23 is included in Section 6. PROM A23 has 256 addressable memory locations (column 1 of Table 4-2). Each memory location contains a 4-bit binary word. The memory locations are addressed by eight address lines A_0–A_7. The status bits are applied to address lines A_4–A_7, and the character position bits are applied to address lines A_0–A_3.

The binary number stored in each memory location is listed in the output column of the table. Only three bits, DO_2–DO_4, are used as the partial address of the character stored in ROM A18. The remaining bit, DO_1, is used otherwise, and its use

Column No.

A23				0			1			2			3			4			5			6			7			8			9			10			11			12			13			14			15		
DO_4	DO_3	DO_2	Row No.	HEX ADRS	HEX DATA	CHAR	HEX ADRS	HEX DATA	CHAR	HEX ADRS	HEX DATA	CHAR	HEX ADRS	HEX DATA	CHAR	HEX ADRS	HEX DATA	CHAR	HEX ADRS	HEX DATA	CHAR	HEX ADRS	HEX DATA	CHAR	HEX ADRS	HEX DATA	CHAR	HEX ADRS	HEX DATA	CHAR	HEX ADRS	HEX DATA	CHAR	HEX ADRS	HEX DATA	CHAR	HEX ADRS	HEX DATA	CHAR	HEX ADRS	HEX DATA	CHAR	HEX ADRS	HEX DATA	CHAR	HEX ADRS	HEX DATA	CHAR	HEX ADRS	HEX DATA	CHAR
0	0	0	0	0000 0000 0001 0000 0002 0000 0003 0000 0004 0000 0005 0000 0006 0000 0007 0000		Δ	0040 0000 0041 0000 0042 0000 0043 0000 0044 0000 0045 0000 0046 0000 0047 0000		Δ	0080 0000 0081 0000 0082 0000 0083 0000 0084 0000 0085 0000 0086 0000 0087 0000		Δ	00C0 0000 00C1 0000 00C2 0000 00C3 0000 00C4 0000 00C5 0000 00C6 0000 00C7 0000		Δ	0100 0000 0101 0000 0102 0000 0103 0000 0104 0000 0105 0000 0106 0000 0107 0000		Δ	0140 0000 0141 0000 0142 0000 0143 0000 0144 0000 0145 0000 0146 0000 0147 0000		Δ	0180 0000 0181 0000 0182 0000 0183 0000 0184 0000 0185 0000 0186 0000 0187 0000		Δ	01C0 0000 01C1 0000 01C2 0000 01C3 0000 01C4 0000 01C5 0000 01C6 0000 01C7 0000		Δ	0200 0000 0201 0000 0202 0000 0203 0000 0204 0000 0205 0000 0206 0000 0207 0000		Δ	0240 0000 0241 0000 0242 0000 0243 0000 0244 0000 0245 0000 0246 0000 0247 0000		Δ	0280 0000 0281 0000 0282 0000 0283 0000 0284 0000 0285 0000 0286 0000 0287 0000		Δ	02C0 0000 02C1 0000 02C2 0000 02C3 0000 02C4 0000 02C5 0000 02C6 0000 02C7 0000		Δ	0300 0000 0301 0000 0302 0000 0303 0000 0304 0000 0305 0000 0306 0000 0307 0000		Δ	0340 0000 0341 0000 0342 0000 0343 0000 0344 0000 0345 0000 0346 0000 0347 0000		Δ	0380 0000 0381 0000 0382 0000 0383 0000 0384 0000 0385 0000 0386 0000 0387 0000		Δ	03C0 0000 03C1 0000 03C2 0000 03C3 0000 03C4 0000 03C5 0000 03C6 0000 03C7 0000		Δ
0	0	1	1	0008 0000 0009 007F 000A 0FFF 000B 027F 000C 021C 000D 021C 000E 021C 000F 001C		T	0048 0000 0049 007F 004A 0FFF 004B 027F 004C 021C 004D 021C 004E 021C 004F 001C		T	0088 0000 0089 007F 008A 0FFF 008B 027F 008C 021C 008D 021C 008E 021C 008F 001C		T	00C8 0000 00C9 007F 00CA 0FFF 00CB 027F 00CC 021C 00CD 021C 00CE 021C 00CF 001C		T	0108 0000 0109 007F 010A 0FFF 010B 027F 010C 021C 010D 021C 010E 021C 010F 001C		T	0148 0000 0149 007F 014A 0FFF 014B 027F 014C 021C 014D 021C 014E 021C 014F 001C		T	0188 0000 0189 007F 018A 0FFF 018B 027F 018C 021C 018D 021C 018E 021C 018F 001C		T	01C8 0000 01C9 007F 01CA 0FFF 01CB 027F 01CC 021C 01CD 021C 01CE 021C 01CF 001C		T	0208 0000 0209 007F 020A 0FFF 020B 027F 020C 021C 020D 021C 020E 021C 020F 001C		T	0248 0000 0249 007F 024A 0FFF 024B 027F 024C 021C 024D 021C 024E 021C 024F 001C		T	0288 0000 0289 007F 028A 0FFF 028B 027F 028C 021C 028D 021C 028E 021C 028F 001C		T	02C8 0000 02C9 007F 02CA 0FFF 02CB 027F 02CC 021C 02CD 021C 02CE 021C 02CF 001C		T	0308 0000 0309 007F 030A 0FFF 030B 027F 030C 021C 030D 021C 030E 021C 030F 001C		T	0348 0000 0349 007F 034A 0FFF 034B 027F 034C 021C 034D 021C 034E 021C 034F 001C		T	0388 0000 0389 007F 038A 0FFF 038B 027F 038C 021C 038D 021C 038E 021C 038F 001C		T	03C8 0000 03C9 007F 03CA 0FFF 03CB 027F 03CC 021C 03CD 021C 03CE 021C 03CF 001C		T
0	1	0	2	0010 0000 0011 000E 0012 011E 0013 031E 0014 011E 0015 011F 0016 039F 0017 001F		1	0050 0000 0051 000E 0052 011E 0053 031E 0054 011E 0055 011F 0056 039F 0057 001F		1	0090 0000 0091 000E 0092 011E 0093 031E 0094 011E 0095 011F 0096 039F 0097 001F		1	00D0 0000 00D1 000E 00D2 011E 00D3 031E 00D4 011E 00D5 011F 00D6 039F 00D7 001F		1	0110 0000 0111 003F 0112 07BF 0113 00BF 0114 07BF 0115 043F 0116 07BF 0117 003F		2	0150 0000 0151 003F 0152 07BF 0153 00BF 0154 07BF 0155 043F 0156 07BF 0157 003F		2	0190 0000 0191 003F 0192 07BF 0193 00BF 0194 07BF 0195 043F 0196 07BF 0197 003F		2	01D0 0000 01D1 003F 01D2 07BF 01D3 00BF 01D4 07BF 01D5 043F 01D6 07BF 01D7 003F		2	0210 0000 0211 003F 0212 07BF 0213 043F 0214 0438 0215 043F 0216 07BF 0217 003F		C	0250 0000 0251 003F 0252 07BF 0253 043F 0254 0438 0255 043F 0256 07BF 0257 003F		C	0290 0000 0291 003F 0292 07BF 0293 043F 0294 0438 0295 043F 0296 07BF 0297 003F		C	02D0 0000 02D1 003F 02D2 07BF 02D3 043F 02D4 0438 02D5 043F 02D6 07BF 02D7 003F		C	0310 0000 0311 003F 0312 07BF 0313 043F 0314 0438 0315 043F 0316 07BF 0317 003F		C	0350 0000 0351 003F 0352 07BF 0353 043F 0354 0438 0355 043F 0356 07BF 0357 003F		C	0390 0000 0391 003F 0392 07BF 0393 043F 0394 0438 0395 043F 0396 07BF 0397 003F		C	03D0 0000 03D1 003F 03D2 07BF 03D3 043F 03D4 0438 03D5 043F 03D6 07BF 03D7 003F		C
0	1	1	3	0018 0000 0019 0000 001A 001C 001B 021C 001C 001C 001D 021C 001E 001C 001F 0000		:	0058 0000 0059 0000 005A 001C 005B 021C 005C 001C 005D 021C 005E 001C 005F 0000		:	0098 0000 0099 0000 009A 0000 009B 0000 009C 0000 009D 0000 009E 0000 009F 0000		Δ	00D8 0000 00D9 0000 00DA 0000 00DB 0000 00DC 0000 00DD 0000 00DE 0000 00DF 0000		Δ	0118 0000 0119 0000 011A 001C 011B 021C 011C 001C 011D 021C 011E 001C 011F 0000		:	0158 0000 0159 0000 015A 001C 015B 021C 015C 001C 015D 021C 015E 001C 015F 0000		:	0198 0000 0199 0000 019A 0000 019B 0000 019C 0000 019D 0000 019E 0000 019F 0000		Δ	01D8 0000 01D9 0000 01DA 0000 01DB 0000 01DC 0000 01DD 0000 01DE 0000 01DF 0000		Δ	0218 0000 0219 0000 021A 001C 021B 021C 021C 001C 021D 021C 021E 001C 021F 0000		:	0258 0000 0259 0000 025A 000E 025B 010E 025C 000E 025D 011E 025E 021E 025F 001C		;	0298 0000 0299 0000 029A 001C 029B 021C 029C 001C 029D 021C 029E 001C 029F 0000		:	02D8 0000 02D9 0000 02DA 000E 02DB 010E 02DC 000E 02DD 011E 02DE 021E 02DF 001C		;	0318 0000 0319 0000 031A 001C 031B 021C 031C 001C 031D 021C 031E 001C 031F 0000		:	0358 0000 0359 0000 035A 000E 035B 010E 035C 000E 035D 011E 035E 021E 035F 001C		;	0398 0000 0399 0000 039A 001C 039B 021C 039C 001C 039D 021C 039E 001C 039F 0000		:	03D8 0000 03D9 0000 03DA 000E 03DB 010E 03DC 000E 03DD 011E 03DE 021E 03DF 001C		;
1	0	0	4	0020 0000 0021 0000 0022 0000 0023 007F 0024 0FFF 0025 007F 0026 0000 0027 0000		-	0060 0000 0061 0000 0062 0000 0063 007F 0064 0FFF 0065 007F 0066 0000 0067 0000		-	00A0 0000 00A1 0000 00A2 0000 00A3 007F 00A4 0FFF 00A5 007F 00A6 0000 00A7 0000		-	00E0 0000 00E1 0000 00E2 0000 00E3 007F 00E4 0FFF 00E5 007F 00E6 0000 00E7 0000		-	0120 0000 0121 0000 0122 0000 0123 007F 0124 0FFF 0125 007F 0126 0000 0127 0000		-	0160 0000 0161 0000 0162 0000 0163 007F 0164 0FFF 0165 007F 0166 0000 0167 0000		-	01A0 0000 01A1 0000 01A2 0000 01A3 007F 01A4 0FFF 01A5 007F 01A6 0000 01A7 0000		-	01E0 0000 01E1 0000 01E2 0000 01E3 007F 01E4 0FFF 01E5 007F 01E6 0000 01E7 0000		-	0220 0000 0221 0000 0222 0000 0223 007F 0224 0FFF 0225 007F 0226 0000 0227 0000		-	0260 0000 0261 0000 0262 0000 0263 007F 0264 0FFF 0265 007F 0266 0000 0267 0000		-	02A0 0000 02A1 0000 02A2 0000 02A3 007F 02A4 0FFF 02A5 007F 02A6 0000 02A7 0000		-	02E0 0000 02E1 0000 02E2 0000 02E3 007F 02E4 0FFF 02E5 007F 02E6 0000 02E7 0000		-	0320 0000 0321 0000 0322 0000 0323 007F 0324 0FFF 0325 007F 0326 0000 0327 0000		-	0360 0000 0361 0000 0362 0000 0363 007F 0364 0FFF 0365 007F 0366 0000 0367 0000		-	03A0 0000 03A1 0000 03A2 0000 03A3 007F 03A4 0FFF 03A5 007F 03A6 0000 03A7 0000		-	03E0 0000 03E1 0000 03E2 0000 03E3 007F 03E4 0FFF 03E5 007F 03E6 0000 03E7 0000		-
1	0	1	5	0028 0000 0029 0000 002A 0000 002B 0000 002C 0000 002D 0000 002E 0000 002F 0000		Δ	0068 0000 0069 0000 006A 0000 006B 0000 006C 0000 006D 0000 006E 0000 006F 0000		Δ	00A8 0000 00A9 0000 00AA 0000 00AB 0000 00AC 0000 00AD 0000 00AE 0000 00AF 0000		Δ	00E8 0000 00E9 0000 00EA 0000 00EB 0000 00EC 0000 00ED 0000 00EE 0000 00EF 0000		Δ	0128 0000 0129 0000 012A 0000 012B 0000 012C 0000 012D 0000 012E 0000 012F 0000		Δ	0168 0000 0169 0000 016A 0000 016B 0000 016C 0000 016D 0000 016E 0000 016F 0000		Δ	01A8 0000 01A9 0000 01AA 0000 01AB 0000 01AC 0000 01AD 0000 01AE 0000 01AF 0000		Δ	01E8 0000 01E9 0000 01EA 0000 01EB 0000 01EC 0000 01ED 0000 01EE 0000 01EF 0000		Δ	0228 0000 0229 0000 022A 0000 022B 0000 022C 0000 022D 0000 022E 0000 022F 0000		Δ	0268 0000 0269 0000 026A 0000 026B 0000 026C 0000 026D 0000 026E 0000 026F 0000		Δ	02A8 0000 02A9 0000 02AA 0000 02AB 0000 02AC 0000 02AD 0000 02AE 0000 02AF 0000		Δ	02E8 0000 02E9 0000 02EA 0000 02EB 0000 02EC 0000 02ED 0000 02EE 0000 02EF 0000		Δ	0328 0000 0329 0000 032A 0000 032B 0000 032C 0000 032D 0000 032E 0000 032F 0000		Δ	0368 0000 0369 0000 036A 0000 036B 0000 036C 0000 036D 0000 036E 0000 036F 0000		Δ	03A8 0000 03A9 0000 03AA 0000 03AB 0000 03AC 0000 03AD 0000 03AE 0000 03AF 0000		Δ	03E8 0000 03E9 0000 03EA 0000 03EB 0000 03EC 0000 03ED 0000 03EE 0000 03EF 0000		Δ
1	1	0	6	0030 0000 0031 003F 0032 07BF 0033 04BF 0034 04BF 0035 04BF 0036 07BF 0037 003F		0	0070 0000 0071 000E 0072 011E 0073 031E 0074 011E 0075 011F 0076 039F 0077 001F		1	00B0 0000 00B1 003F 00B2 07BF 00B3 00BF 00B4 07BF 00B5 043F 00B6 07BF 00B7 003F		2	00F0 0000 00F1 003F 00F2 07BF 00F3 00BF 00F4 039F 00F5 00BF 00F6 07BF 00F7 003F		3	0130 0000 0131 003E 0132 053E 0133 053F 0134 07BF 0135 013F 0136 010E 0137 000E		4	0170 0000 0171 003F 0172 07BF 0173 043F 0174 07BF 0175 00BF 0176 07BF 0177 003F		5	01B0 0000 01B1 003E 01B2 073E 01B3 043F 01B4 07BF 01B5 04BF 01B6 07BF 01B7 003F		6	01F0 0000 01F1 003F 01F2 07BF 01F3 00BF 01F4 0087 01F5 0087 01F6 0087 01F7 0007		7	0230 0000 0231 003F 0232 07BF 0233 04BF 0234 07BF 0235 04BF 0236 07BF 0237 003F		8	0270 0000 0271 003F 0272 07BF 0273 04BF 0274 07BF 0275 00BF 0276 039F 0277 001F		9	02B0 0000 02B1 003F 02B2 07BF 02B3 04BF 02B4 07BF 02B5 04BF 02B6 04BF 02B7 003F		A	02F0 0000 02F1 007F 02F2 0FFF 02F3 04FF 02F4 07BF 02F5 04FF 02F6 0FFF 02F7 007F		B	0330 0000 0331 003F 0332 07BF 0333 043F 0334 0438 0335 043F 0336 07BF 0337 003F		C	0370 0000 0371 007F 0372 0FFF 0373 04FF 0374 04BF 0375 04FF 0376 0FFF 0377 007F		D	03B0 0000 03B1 003F 03B2 07BF 03B3 043F 03B4 073E 03B5 043F 03B6 07BF 03B7 003F		E	03F0 0000 03F1 003F 03F2 07BF 03F3 043F 03F4 073E 03F5 043E 03F6 0438 03F7 0038		F
1	1	1	7	0038 0000 0039 0000 003A 001C 003B 021C 003C 001C 003D 021C 003E 001C 003F 0000		:	0078 0000 0079 0000 007A 001C 007B 021C 007C 001C 007D 021C 007E 001C 007F 0000		:	00B8 0000 00B9 0000 00BA 001C 00BB 021C 00BC 001C 00BD 021C 00BE 001C 00BF 0000		:	00F8 0000 00F9 0000 00FA 001C 00FB 021C 00FC 001C 00FD 021C 00FE 001C 00FF 0000		:	0138 0000 0139 0000 013A 001C 013B 021C 013C 001C 013D 021C 013E 001C 013F 0000		:	0178 0000 0179 0000 017A 001C 017B 021C 017C 001C 017D 021C 017E 001C 017F 0000		:	01B8 0000 01B9 0000 01BA 001C 01BB 021C 01BC 001C 01BD 021C 01BE 001C 01BF 0000		:	01F8 0000 01F9 0000 01FA 001C 01FB 021C 01FC 001C 01FD 021C 01FE 001C 01FF 0000		:	0238 0000 0239 0000 023A 001C 023B 021C 023C 001C 023D 021C 023E 001C 023F 0000		:	0278 0000 0279 0000 027A 000E 027B 010E 027C 000E 027D 011E 027E 021E 027F 001C		;	02B8 0000 02B9 0000 02BA 001C 02BB 021C 02BC 001C 02BD 021C 02BE 001C 02BF 0000		:	02F8 0000 02F9 0000 02FA 000E 02FB 010E 02FC 000E 02FD 011E 02FE 021E 02FF 001C		;	0338 0000 0339 0000 033A 001C 033B 021C 033C 001C 033D 021C 033E 001C 033F 0000		:	0378 0000 0379 0000 037A 000E 037B 010E 037C 000E 037D 011E 037E 021E 037F 001C		;	03B8 0000 03B9 0000 03BA 001C 03BB 021C 03BC 001C 03BD 021C 03BE 001C 03BF 0000		:	03F8 0000 03F9 0000 03FA 001C 03FB 021C 03FC 001C 03FD 023C 03FE 043C 03FF 0038		:

NOTE: DELTA (Δ) INDICATES A BLANK

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Table 4-1.
Contents of ROM A18

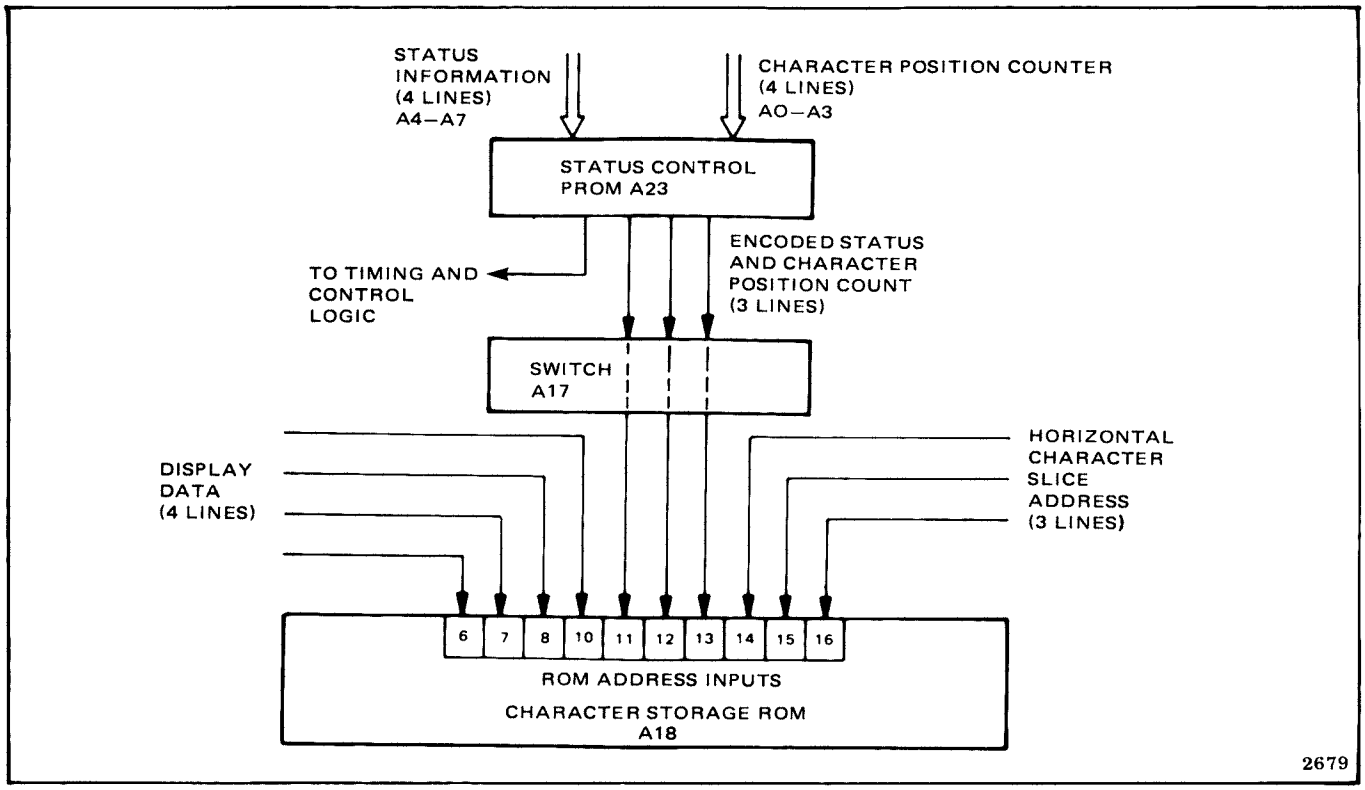

Figure 4-7. Character Addressing

is not relevant to the present discussion. (See paragraph 4-12.) The decimal equivalent of the three-bit binary number, DO_2–DO_4, is listed in the right-hand column of Table 4-2. (DO_4 is the most significant bit.) This number is the address of the characters in the row of the same number listed in Table 4-1. As an example, when PROM A23 puts out 000 (decimal 0) at pins DO_4 through DO_2 (see Table 4-2), the characters addressed by this partial address can be seen in row 0 of Table 4-1, and in this case all sixteen of the character locations are blank. As another example, when ROM A23 puts out 001 (decimal 1) at pins DO_4 through DO_2 (see Table 4-2), the characters addressed by this partial address can be seen in row 1 of Table 4-1. In this case, all sixteen of the character locations contain the letter "T".

When Table 4-2 is examined it can be seen that every entry in this table for character position bit indications of 3 and 15 addresses the characters contained in row 0 of Table 4-1. The characters in row 0 are all blank. This is compatible with Figure 4-3 which shows character positions 3 and 15 always blank (regardless of status information). Similarly, Table 4-2 shows that when the character position address lines have a decimal value 1, the characters in row 1 of Table 4-1 are selected. The characters in row 1 of Table 4-1 are all the letter "T". This is compatible with Figure 4-3 which shows that the character displayed in position 1 is always the letter "T", regardless of status information.

Figure 4-3 indicates that numerals are always required in character positions 4, 5, 7, 8, 10, 11, 13, and 14. Table 4-1 indicates that all of the required numerals are located in row 6. Referring to Table 4-2, whenever the character position decimal is 4, 5, 7, 8, 10, 11, 13, or 14, the row number of the characters addressed is 6.

When the numerals in row 6 of Table 4-1 are selected (by character position and status information) the data lines from the tape time data storage RAM A12 select one of the 16 columns of characters. At the intersection of the row and column is found the numeral that will be displayed.

Table 4-2. Contents of PROM A23

PROM A23 ADDRESS										PROM A23 OUTPUT					
DECIMAL	HEX	BINARY								BINARY				HEX	ROW NO. OF DATA ADDRESSED IN ROM A18 (SEE TABLE 4-1)
		STATUS BITS				CHARACTER POSITION BITS									
		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	DO_4	DO_3	DO_2	DO_1		
000	00	0	0	0	0	0	0	0	0	0	0	1	0	2	1
001	01	0	0	0	0	0	0	0	1	0	0	0	0	0	0
002	02	0	0	0	0	0	0	1	0	0	1	0	0	4	2
003	03	0	0	0	0	0	0	1	1	0	0	0	0	0	0
004	04	0	0	0	0	0	1	0	0	1	1	0	1	D	6
005	05	0	0	0	0	0	1	0	1	1	1	0	1	D	6
006	06	0	0	0	0	0	1	1	0	0	0	0	0	0	0
007	07	0	0	0	0	0	1	1	1	1	1	0	1	D	6
008	08	0	0	0	0	1	0	0	0	1	1	0	1	D	6
009	09	0	0	0	0	1	0	0	1	0	0	0	0	0	0
010	0A	0	0	0	0	1	0	1	0	1	1	0	1	D	6
011	0B	0	0	0	0	1	0	1	1	1	1	0	1	D	6
012	0C	0	0	0	0	1	1	0	0	0	0	0	0	0	0
013	0D	0	0	0	0	1	1	0	1	1	1	0	1	D	6
014	0E	0	0	0	0	1	1	1	0	1	1	0	1	D	6
015	0F	0	0	0	0	1	1	1	1	0	0	0	0	0	0
016	10	0	0	0	1	0	0	0	0	0	0	1	0	2	1
017	11	0	0	0	1	0	0	0	1	0	0	1	0	2	1
018	12	0	0	0	1	0	0	1	0	0	1	0	0	4	2
019	13	0	0	0	1	0	0	1	1	0	0	0	0	0	0
020	14	0	0	0	1	0	1	0	0	1	1	0	1	D	6
021	15	0	0	0	1	0	1	0	1	1	1	0	1	D	6
022	16	0	0	0	1	0	1	1	0	0	0	0	0	0	0
023	17	0	0	0	1	0	1	1	1	1	1	0	1	D	6
024	18	0	0	0	1	1	0	0	0	1	1	0	1	D	6
025	19	0	0	0	1	1	0	0	1	0	0	0	0	0	0
026	1A	0	0	0	1	1	0	1	0	1	1	0	1	D	6
027	1B	0	0	0	1	1	0	1	1	1	1	0	1	D	6
028	1C	0	0	0	1	1	1	0	0	0	0	0	0	0	0
029	1D	0	0	0	1	1	1	0	1	1	1	0	1	D	6
030	1E	0	0	0	1	1	1	1	0	1	1	0	1	D	6
031	1F	0	0	0	1	1	1	1	1	0	0	0	0	0	0

Table 4-2. Contents of PROM A23 (Continued)

DECIMAL	HEX	PROM A23 ADDRESS								PROM A23 OUTPUT					ROW NO. OF DATA ADDRESSED IN ROM A18 (SEE TABLE 4-1)
		BINARY								BINARY				HEX	
		STATUS BITS				CHARACTER POSITION BITS									
		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	DO_4	DO_3	DO_2	DO_1		
032	20	0	0	1	0	0	0	0	0	0	0	1	0	2	1
033	21	0	0	1	0	0	0	0	1	0	1	0	0	4	2
034	22	0	0	1	0	0	0	1	0	0	1	0	0	4	2
035	23	0	0	1	0	0	0	1	1	0	0	0	0	0	0
036	24	0	0	1	0	0	1	0	0	1	1	0	1	D	6
037	25	0	0	1	0	0	1	0	1	1	1	0	1	D	6
038	26	0	0	1	0	0	1	1	0	0	0	0	0	0	0
039	27	0	0	1	0	0	1	1	1	1	1	0	1	D	6
040	28	0	0	1	0	1	0	0	0	1	1	0	1	D	6
041	29	0	0	1	0	1	0	0	1	0	0	0	0	0	0
042	2A	0	0	1	0	1	0	1	0	1	1	0	1	D	6
043	2B	0	0	1	0	1	0	1	1	1	1	0	1	D	6
044	2C	0	0	1	0	1	1	0	0	0	0	0	0	0	0
045	2D	0	0	1	0	1	1	0	1	1	1	0	1	D	6
046	2E	0	0	1	0	1	1	1	0	1	1	0	1	D	6
047	2F	0	0	1	0	1	1	1	1	0	0	0	0	0	0
048	30	0	0	1	1	0	0	0	0	0	0	1	0	2	1
049	31	0	0	1	1	0	0	0	1	0	1	0	0	4	2
050	32	0	0	1	1	0	0	1	0	0	1	0	0	4	2
051	33	0	0	1	1	0	0	1	1	0	0	0	0	0	0
052	34	0	0	1	1	0	1	0	0	1	1	0	1	D	6
053	35	0	0	1	1	0	1	0	1	1	1	0	1	D	6
054	36	0	0	1	1	0	1	1	0	0	0	0	0	0	0
055	37	0	0	1	1	0	1	1	1	1	1	0	1	D	6
056	38	0	0	1	1	1	0	0	0	1	1	0	1	D	6
057	39	0	0	1	1	1	0	0	1	0	0	0	0	0	0
058	3A	0	0	1	1	1	0	1	0	1	1	0	1	D	6
059	3B	0	0	1	1	1	0	1	1	1	1	0	1	D	6
060	3C	0	0	1	1	1	1	0	0	0	0	0	0	0	0
061	3D	0	0	1	1	1	1	0	1	1	1	0	1	D	6
062	3E	0	0	1	1	1	1	1	0	1	1	0	1	D	6
063	3F	0	0	1	1	1	1	1	1	0	0	0	0	0	0

Table 4-2. Contents of PROM A23 (Continued)

DECIMAL	HEX	PROM A23 ADDRESS								PROM A23 OUTPUT				HEX	ROW NO. OF DATA ADDRESSED IN ROM A18 (SEE TABLE 4-1)
		BINARY								BINARY					
		STATUS BITS				CHARACTER POSITION BITS									
		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	DO_4	DO_3	DO_2	DO_1		
064	40	0	1	0	0	0	0	0	0	0	0	1	0	2	1
065	41	0	1	0	0	0	0	0	1	0	0	0	0	0	0
066	42	0	1	0	0	0	0	1	0	0	0	0	0	0	0
067	43	0	1	0	0	0	0	1	1	0	0	0	0	0	0
068	44	0	1	0	0	0	1	0	0	1	1	0	1	D	6
069	45	0	1	0	0	0	1	0	1	1	1	0	1	D	6
070	46	0	1	0	0	0	1	1	0	0	0	0	0	0	0
071	47	0	1	0	0	0	1	1	1	1	1	0	1	D	6
072	48	0	1	0	0	1	0	0	0	1	1	0	1	D	6
073	49	0	1	0	0	1	0	0	1	0	0	0	0	0	0
074	4A	0	1	0	0	1	0	1	0	1	1	0	1	D	6
075	4B	0	1	0	0	1	0	1	1	1	1	0	1	D	6
076	4C	0	1	0	0	1	1	0	0	0	0	0	0	0	0
077	4D	0	1	0	0	1	1	0	1	1	1	0	1	D	6
078	4E	0	1	0	0	1	1	1	0	1	1	0	1	D	6
079	4F	0	1	0	0	1	1	1	1	0	0	0	0	0	0
080	50	0	1	0	1	0	0	0	0	0	0	1	0	2	1
081	51	0	1	0	1	0	0	0	1	0	0	1	0	2	1
082	52	0	1	0	1	0	0	1	0	0	0	0	0	0	0
083	53	0	1	0	1	0	0	1	1	0	0	0	0	0	0
084	54	0	1	0	1	0	1	0	0	1	1	0	1	D	6
085	55	0	1	0	1	0	1	0	1	1	1	0	1	D	6
086	56	0	1	0	1	0	1	1	0	0	0	0	0	0	0
087	57	0	1	0	1	0	1	1	1	1	1	0	1	D	6
088	58	0	1	0	1	1	0	0	0	1	1	0	1	D	6
089	59	0	1	0	1	1	0	0	1	0	0	0	0	0	0
090	5A	0	1	0	1	1	0	1	0	1	1	0	1	D	6
091	5B	0	1	0	1	1	0	1	1	1	1	0	1	D	6
092	5C	0	1	0	1	1	1	0	0	0	0	0	0	0	0
093	5D	0	1	0	1	1	1	0	1	1	1	0	1	D	6
094	5E	0	1	0	1	1	1	1	0	1	1	0	1	D	6
095	5F	0	1	0	1	1	1	1	1	0	0	0	0	0	0

Table 4-2. Contents of PROM A23 (Continued)

DECIMAL	HEX	PROM A23 ADDRESS								PROM A23 OUTPUT					ROW NO. OF DATA ADDRESSED IN ROM A18 (SEE TABLE 4-1)
		BINARY								BINARY				HEX	
		STATUS BITS				CHARACTER POSITION BITS									
		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	DO_4	DO_3	DO_2	DO_1		
096	60	0	1	1	0	0	0	0	0	0	0	1	0	2	1
097	61	0	1	1	0	0	0	0	1	0	1	0	0	4	2
098	62	0	1	1	0	0	0	1	0	0	0	0	0	0	0
099	63	0	1	1	0	0	0	1	1	0	0	0	0	0	0
100	64	0	1	1	0	0	1	0	0	1	1	0	1	D	6
101	65	0	1	1	0	0	1	0	1	1	1	0	1	D	6
102	66	0	1	1	0	0	1	1	0	0	0	0	0	0	0
103	67	0	1	1	0	0	1	1	1	1	1	0	1	D	6
104	68	0	1	1	0	1	0	0	0	1	1	0	1	D	6
105	69	0	1	1	0	1	0	0	1	0	0	0	0	0	0
106	6A	0	1	1	0	1	0	1	0	1	1	0	1	D	6
107	6B	0	1	1	0	1	0	1	1	1	1	0	1	D	6
108	6C	0	1	1	0	1	1	0	0	0	0	0	0	0	0
109	6D	0	1	1	0	1	1	0	1	1	1	0	1	D	6
110	6E	0	1	1	0	1	1	1	0	1	1	0	1	D	6
111	6F	0	1	1	0	1	1	1	1	0	0	0	0	0	0
112	70	0	1	1	1	0	0	0	0	0	0	1	0	2	1
113	71	0	1	1	1	0	0	0	1	0	1	0	0	4	2
114	72	0	1	1	1	0	0	1	0	0	0	0	0	0	0
115	73	0	1	1	1	0	0	1	1	0	0	0	0	0	0
116	74	0	1	1	1	0	1	0	0	1	1	0	1	D	6
117	75	0	1	1	1	0	1	0	1	1	1	0	1	D	6
118	76	0	1	1	1	0	1	1	0	0	0	0	0	0	0
119	77	0	1	1	1	0	1	1	1	1	1	0	1	D	6
120	78	0	1	1	1	1	0	0	0	1	1	0	1	D	6
121	79	0	1	1	1	1	0	0	1	0	0	0	0	0	0
122	7A	0	1	1	1	1	0	1	0	1	1	0	1	D	6
123	7B	0	1	1	1	1	0	1	1	1	1	0	1	D	6
124	7C	0	1	1	1	1	1	0	0	0	0	0	0	0	0
125	7D	0	1	1	1	1	1	0	1	1	1	0	1	D	6
126	7E	0	1	1	1	1	1	1	0	1	1	0	1	D	6
127	7F	0	1	1	1	1	1	1	1	0	0	0	0	0	0

Table 4-2. Contents of PROM A23 (Continued)

DECIMAL	HEX	PROM A23 ADDRESS								PROM A23 OUTPUT					ROW NO. OF DATA ADDRESSED IN ROM A18 (SEE TABLE 4-1)
		BINARY								BINARY				HEX	
		STATUS BITS				CHARACTER POSITION BITS									
		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	DO_4	DO_3	DO_2	DO_1		
128	80	1	0	0	0	0	0	0	0	0	0	1	0	2	1
129	81	1	0	0	0	0	0	0	1	0	0	0	0	0	0
130	82	1	0	0	0	0	0	1	0	0	1	0	0	4	2
131	83	1	0	0	0	0	0	1	1	0	0	0	0	0	0
132	84	1	0	0	0	0	1	0	0	1	1	0	1	0	6
133	85	1	0	0	0	0	1	0	1	1	1	0	1	D	6
134	86	1	0	0	0	0	1	1	0	0	1	1	0	6	3
135	87	1	0	0	0	0	1	1	1	1	1	0	1	D	6
136	88	1	0	0	0	1	0	0	0	1	1	0	1	D	6
137	89	1	0	0	0	1	0	0	1	0	1	1	0	6	3
138	8A	1	0	0	0	1	0	1	0	1	1	0	1	D	6
139	8B	1	0	0	0	1	0	1	1	1	1	0	1	D	6
140	8C	1	0	0	0	1	1	0	0	0	1	1	0	6	3
141	8D	1	0	0	0	1	1	0	1	1	1	0	1	D	6
142	8E	1	0	0	0	1	1	1	0	1	1	0	1	D	6
143	8F	1	0	0	0	1	1	1	1	0	0	0	0	0	0
144	90	1	0	0	1	0	0	0	0	0	0	1	0	2	1
145	91	1	0	0	1	0	0	0	1	0	0	1	0	2	1
146	92	1	0	0	1	0	0	1	0	0	1	0	0	4	2
147	93	1	0	0	1	0	0	1	1	0	0	0	0	0	0
148	94	1	0	0	1	0	1	0	0	1	1	0	1	D	6
149	95	1	0	0	1	0	1	0	1	1	1	0	1	D	6
150	96	1	0	0	1	0	1	1	0	0	1	1	0	6	3
151	97	1	0	0	1	0	1	1	1	1	1	0	1	D	6
152	98	1	0	0	1	1	0	0	0	1	1	0	1	D	6
153	99	1	0	0	1	1	0	0	1	0	1	1	0	6	3
154	9A	1	0	0	1	1	0	1	0	1	1	0	1	D	6
155	9B	1	0	0	1	1	0	1	1	1	1	0	1	D	6
156	9C	1	0	0	1	1	1	0	0	0	1	1	0	6	3
157	9D	1	0	0	1	1	1	0	1	1	1	0	1	D	6
158	9E	1	0	0	1	1	1	1	0	1	1	0	1	D	6
159	9F	1	0	0	1	1	1	1	1	0	0	0	0	0	0

Table 4-2. Contents of PROM A23 (Continued)

DECIMAL	HEX	PROM A23 ADDRESS								PROM A23 OUTPUT					ROW NO. OF DATA ADDRESSED IN ROM A18 (SEE TABLE 4-1)
		BINARY								BINARY				HEX	
		STATUS BITS				CHARACTER POSITION BITS									
		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	DO_4	DO_3	DO_2	DO_1		
160	A 0	1	0	1	0	0	0	0	0	0	0	1	0	2	1
161	A 1	1	0	1	0	0	0	0	1	0	1	0	0	4	2
162	A 2	1	0	1	0	0	0	1	0	0	1	0	0	4	2
163	A 3	1	0	1	0	0	0	1	1	0	0	0	0	0	0
164	A 4	1	0	1	0	0	1	0	0	1	1	0	1	D	6
165	A 5	1	0	1	0	0	1	0	1	1	1	0	1	D	6
166	A 6	1	0	1	0	0	1	1	0	0	1	1	0	6	3
167	A 7	1	0	1	0	0	1	1	1	1	1	0	1	D	6
168	A 8	1	0	1	0	1	0	0	0	1	1	0	1	D	6
169	A 9	1	0	1	0	1	0	0	1	0	1	1	0	6	3
170	A A	1	0	1	0	1	0	1	0	1	1	0	1	D	6
171	A B	1	0	1	0	1	0	1	1	1	1	0	1	D	6
172	A C	1	0	1	0	1	1	0	0	0	1	1	0	6	3
173	A D	1	0	1	0	1	1	0	1	1	1	0	1	D	6
174	A E	1	0	1	0	1	1	1	0	1	1	0	1	D	6
175	A F	1	0	1	0	1	1	1	1	0	0	0	0	0	0
176	B 0	1	0	1	1	0	0	0	0	0	0	1	0	2	1
177	B 1	1	0	1	1	0	0	0	1	0	1	0	0	4	2
178	B 2	1	0	1	1	0	0	1	0	0	1	0	0	4	2
179	B 3	1	0	1	1	0	0	1	1	0	0	0	0	0	0
180	B 4	1	0	1	1	0	1	0	0	1	1	0	1	D	6
181	B 5	1	0	1	1	0	1	0	1	1	1	0	1	D	6
182	B 6	1	0	1	1	0	1	1	0	0	1	1	0	6	3
183	B 7	1	0	1	1	0	1	1	1	1	1	0	1	D	6
184	B 8	1	0	1	1	1	0	0	0	1	1	0	1	D	6
185	B 9	1	0	1	1	1	0	0	1	0	1	1	0	6	3
186	B A	1	0	1	1	1	0	1	0	1	1	0	1	D	6
187	B B	1	0	1	1	1	0	1	1	1	1	0	1	D	6
188	B C	1	0	1	1	1	1	0	0	0	1	1	0	6	3
189	B D	1	0	1	1	1	1	0	1	1	1	0	1	D	6
190	B E	1	0	1	1	1	1	1	0	1	1	0	1	D	6
191	B F	1	0	1	1	1	1	1	1	0	0	0	0	0	0

Table 4-2. Contents of PROM A23 (Continued)

DECIMAL	HEX	PROM A23 ADDRESS								PROM A23 OUTPUT					ROW NO. OF DATA ADDRESSED IN ROM A18 (SEE TABLE 4-1)
		BINARY								BINARY				HEX	
		STATUS BITS				CHARACTER POSITION BITS									
		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	DO_4	DO_3	DO_2	DO_1		
192	C 0	1	1	0	0	0	0	0	0	0	0	1	0	2	1
193	C 1	1	1	0	0	0	0	0	1	0	0	0	0	0	0
194	C 2	1	1	0	0	0	0	1	0	0	1	0	0	4	2
195	C 3	1	1	0	0	0	0	1	1	0	0	0	0	0	0
196	C 4	1	1	0	0	0	1	0	0	1	1	0	1	D	6
197	C 5	1	1	0	0	0	1	0	1	1	1	0	1	D	6
198	C 6	1	1	0	0	0	1	1	0	0	1	1	0	6	3
199	C 7	1	1	0	0	0	1	1	1	1	1	0	1	D	6
200	C 8	1	1	0	0	1	0	0	0	1	1	0	1	D	6
201	C 9	1	1	0	0	1	0	0	1	0	1	1	0	6	3
202	C A	1	1	0	0	1	0	1	0	1	1	0	1	D	6
203	C B	1	1	0	0	1	0	1	1	1	1	0	1	D	6
204	C C	1	1	0	0	1	1	0	0	0	1	1	0	6	3
205	C D	1	1	0	0	1	1	0	1	1	1	0	1	D	6
206	C E	1	1	0	0	1	1	1	0	1	1	0	1	D	6
207	C F	1	1	0	0	1	1	1	1	0	0	0	0	0	0
208	D 0	1	1	0	1	0	0	0	0	0	0	1	0	2	1
209	D 1	1	1	0	1	0	0	0	1	0	0	1	0	2	1
211	D 2	1	1	0	1	0	0	1	0	0	1	0	0	4	2
211	D 3	1	1	0	1	0	0	1	1	0	0	0	0	0	0
212	D 4	1	1	0	1	0	1	0	0	1	1	0	1	D	6
213	D 5	1	1	0	1	0	1	0	1	1	1	0	1	D	6
214	D 6	1	1	0	1	0	1	1	0	0	1	1	0	6	3
215	D 7	1	1	0	1	0	1	1	1	1	1	0	1	D	6
216	D 8	1	1	0	1	1	0	0	0	1	1	0	1	D	6
217	D 9	1	1	0	1	1	0	0	1	0	1	1	0	6	3
218	D A	1	1	0	1	1	0	1	0	1	1	0	1	D	6
219	D B	1	1	0	1	1	0	1	1	1	1	0	1	D	6
220	D C	1	1	0	1	1	1	0	0	0	1	1	0	6	3
221	D D	1	1	0	1	1	1	0	1	1	1	0	1	D	6
222	D E	1	1	0	1	1	1	1	0	1	1	0	1	D	6
223	D F	1	1	0	1	1	1	1	1	0	0	0	0	0	0

Table 4-2. Contents of PROM A23 (Continued)

DECIMAL	HEX	PROM A23 ADDRESS								PROM A23 OUTPUT					ROW NO. OF DATA ADDRESSED IN ROM A18 (SEE TABLE 4-1)
		BINARY								BINARY				HEX	
		STATUS BITS				CHARACTER POSITION BITS									
		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	DO_4	DO_3	DO_2	DO_1		
224	E 0	1	1	1	0	0	0	0	0	0	0	1	0	2	1
225	E 1	1	1	1	0	0	0	0	1	0	1	0	0	4	2
226	E 2	1	1	1	0	0	0	1	0	0	1	0	0	4	2
227	E 3	1	1	1	0	0	0	1	1	0	0	0	0	0	0
228	E 4	1	1	1	0	0	1	0	0	1	1	0	1	D	6
229	E 5	1	1	1	0	0	1	0	1	1	1	0	1	D	6
230	E 6	1	1	1	0	0	1	1	0	0	1	1	0	6	3
231	E 7	1	1	1	0	0	1	1	1	1	1	0	1	D	6
232	E 8	1	1	1	0	1	0	0	0	1	1	0	1	D	6
233	E 9	1	1	1	0	1	0	0	1	0	1	1	0	6	3
234	E A	1	1	1	0	1	0	1	0	1	1	0	1	D	6
235	E B	1	1	1	0	1	0	1	1	1	1	0	1	D	6
236	E C	1	1	1	0	1	1	0	0	0	1	1	0	6	3
237	E D	1	1	1	0	1	1	0	1	1	1	0	1	D	6
238	E E	1	1	1	0	1	1	1	0	1	1	0	1	D	6
239	E F	1	1	1	0	1	1	1	1	0	0	0	0	0	0
240	F 0	1	1	1	1	0	0	0	0	0	0	1	0	2	1
241	F 1	1	1	1	1	0	0	0	1	0	1	0	0	4	2
242	F 2	1	1	1	1	0	0	1	0	0	1	0	0	4	2
243	F 3	1	1	1	1	0	0	1	1	0	0	0	0	0	0
244	F 4	1	1	1	1	0	1	0	0	1	1	0	1	0	1
245	F 5	1	1	1	1	0	1	0	1	1	1	0	1	D	6
246	F 6	1	1	1	1	0	1	1	0	0	1	1	0	6	3
247	F 7	1	1	1	1	0	1	1	1	1	1	0	1	D	6
248	F 8	1	1	1	1	1	0	0	0	1	1	0	1	D	6
249	F 9	1	1	1	1	1	0	0	1	0	1	1	0	6	3
250	F A	1	1	1	1	1	0	1	0	1	1	0	1	D	6
251	F B	1	1	1	1	1	0	1	1	1	1	0	1	D	6
252	F C	1	1	1	1	1	1	0	0	0	1	1	0	6	3
253	F D	1	1	1	1	1	1	0	1	1	1	0	1	D	6
254	F E	1	1	1	1	1	1	1	0	1	1	0	1	D	6
255	F F	1	1	1	1	1	1	1	1	0	0	0	0	0	0

The four data lines from the RAM A12 carry the number to be displayed in BCD format.

When character positions other than those displaying time data are active, status information switch A11 is enabled (time data is disabled). The status information from status logic circuits A8, A21, A28, A29 is entered on the character storage ROM A18 address lines. The column of characters (Table 4-1) chosen depends only on status information. For example, when the characters of row 2 of Table 4-1 are enabled (for character position 2), status information switch A11 is enabled. Status information determines which column is selected and whether a 1 (for tape timer 1) or a 2 (for tape timer 2) is displayed.

Each of the eight individual memory locations within a memory block containing a character is addressed by the three bits produced by the character slice address former (A16). The character slice address former is a counter that produces a binary count ranging from 1 to 7. When the counter produces a 1, the topmost horizontal slice of the character about to be displayed is addressed. At the count of 7, the bottom slice of the character is addressed.

4-7. Vertical Internal Detector, Frame Pulse Detector, H-Pulse Generator Circuit

The vertical interval detector, frame pulse detector, H-pulse generator circuit A49, A48, A47 examines the sync pulses on the incoming composite video and produces vertical interval pulses, frame pulses, and H-pulses required by other circuits on the PWA. The vertical interval detector, frame pulse detector, and H-pulse generator circuit receive composite video that has been stripped of its chrominance, burst, and luminance information. Burst and chrominance are removed by the low-pass filter circuit, L5, C4, C46, R68 and R67. Luminance information is removed by voltage comparator A50, R63, and R64. In addition, the sync pulses remaining are converted from $\overline{\text{T}}$TL to CMOS levels by level translator Q6 before being applied to the vertical internal detector.

One-shot A49-13 is a 3.5-μs one-shot used to detect vertical interval equalizing pulses. Normal sync pulses are 4.7 μs long but equalizing pulses are only 2.3 μs long. Normally, A49-13 will go high on the leading edge of a sync pulse but return low before the trailing edge of the sync pulse can clock D flip-flop A48-1 high. The trailing edge of an equalizing pulse, however, arrives while A49-13 is still high. This clocks a high into A48-1. One-shot A49-5 is a 50-μs one-shot triggered by the trailing edge of A49-4, but only on full-line intervals. If an equalizing pulse arrives at a half-line time, it will be ignored by A49-5. When pin A48-1 goes high it will clock A48-12 low only if it occurred at a full-line interval. One-shot A47-6 will go high whether or not flip-flop A48-12 was low for 720 μs, inhibiting any further action by A48-1 for the rest of the vertical interval. One-shot A47-10 produces shortened H-pulses.

The AND gate A39-10 detects the vertical pulse associated with the tape edit pulse. This pulse is used by the Character Generator PWA to trigger the changing of the display.

4-8. Vertical and Horizontal Position One-Shots

The vertical interval pulse produced by one-shot A47-6 triggers vertical position one-shot A7-5. The delay provided by this circuit determines where the top part of the characters will be positioned vertically on the screen. The VERT POSITION potentiometer R2 on the front of the PWA is in the timing circuit of this one-shot and is used to adjust the vertical positioning of the display.

When vertical position one-shot A7-5 times out and A47-10 goes high, horizontal position one-shot A7-4 is triggered. The delay provided by the horizontal position one-shot circuit determines where the left side of the tape time display will be positioned on the screen. The HORIZ POSITION potentiometer R1 on the front of the PWA is in the timing circuit of this one-shot and is used to adjust the horizontal positioning of the display. The delay of one-shot A7-4 is also adjustable via the CHAR SIZE rotary switch on the front of the PWA which selects resistors R4, R5, or both, to be switched into the timing circuit by switch A1. This gives potentiometer R1 less control as the character size is increased.

4-9. Master Reset Logic

The master reset logic is composed of NOR latch A9-4, A9-3, and AND gate A8-3. It resets the character position counter A31. It also holds the shift clock oscillator off and initializes the timing and control circuit. The master reset pulse begins on receipt of the vertical position one-shot delay pulse and is released when the horizontal position one-shot times out to enable the character display circuitry. The high going vertical position pulse at one-shot A7-5 puts cross-coupled latch A9-3, -4 low, causing gate A8-3, the master reset line, to go low, clearing A3, A21, and A31. The trailing edge of the vertical position pulse enables horizontal position one-shot A7-13. The next H-pulse (A47-10) triggers A7-13 high. This returns gate A8-3 output to high and ends the master reset pulse. After the master reset pulse is removed, characters are displayed on the screen. Before the master reset pulse is removed, character and configuration data are received and stored in RAM A12 for use later in the frame.

4-10. Character Size Selection

The horizontal character slice address former A16 is incremented by pulses from frequency divider A15. The pulses generated by frequency divider A15 are produced by dividing H-pulses by 1, 2, 3, or 4, depending upon the setting of the CHAR SIZE switch. Division of the H-pulses permits the same horizontal slice of the character stored in the ROM to be addressed and read out repeatedly on succeeding lines of a field. When the CHAR SIZE rotary switch is set to 1 (SMALL), the smallest characters are produced. Frequency divider A15 divides the H-pulses by one and each horizontal slice of the character is presented on only one line of a field. Since the raster comprises two interlaced fields and the character slice address former A16 is reset at every vertical interval, a horizontal slice occupies two lines of the raster when the smallest characters are displayed. See Figure 4-1. When medium/small characters are selected the H-pulses are divided by two and the same horizontal slice of a character appears on four succeeding lines of the raster. The horizontal slice of large characters occupies six lines of the raster. In 625-line standards, the characters occupy 4, 6, or 8 raster lines.

The frequency of the clock pulse that shifts the data out of the character data and border data shift registers A4 and A25, determines the horizontal length of the character elements and therefore the character width. The clock pulse is developed by frequency divider A3 operating on the output of oscillator A10, A33, A3, A44, Q1, Q2, Q7, L3, C32, and C33. The oscillator operates at 7-8 MHz and is also divided by 1, 2, 3, or 4 in 525-line standards or by 2, 3, 4, or 5 in 625-line standards to produce small, medium/small, medium, or large characters.

4-11. Anti-Jitter Circuit

The anti-jitter circuit prevents the on-screen time display from visibly jittering up and down between horizontal scan lines of the raster. Jittering could otherwise occur due to the drifting of the time out of the vertical position one-shot A7-5. If the nominal timing out of the vertical interval one-shot occurred close to the arrival of an H-pulse, or close to the beginning of a new horizontal line, fluctuation of the one-shot time out interval could cause disturbance of the display. The display could begin first on one line and then later on a previous or following line, depending on the direction of drift. The anti-jitter circuit eliminates this possibility by changing the time-out interval of the vertical position one-shot by about one quarter of a line whenever the occurrence of the vertical position one-shot time out is close to the arrival of an H-pulse.

Whenever the time out of the vertical position one-shot A7-5 occurs close to the arrival of an H-pulse resistor R3 is added to or subtracted from the timing circuit of one-shot A7-5 by switch A1-1, under the control of toggle flip-flop A35-2. Resistor R3 adds about 15 μs to the time-out of one-shot A7-5. Immediately following the timing out of one-shot A7-5 after a vertical interval, pins 3 and 5 of AND gate A37-9 are high.

Pin A37-1 is held high by A7-12 until the next vertical interval. Pin A37-8 is held high only for the short duration determined by the pulse delay circuit composed of R33 and C23. If the high going H-pulse is applied to pin A37-2 within the time frame determined by the pulse delay circuit, pin A37-9 goes high. This toggles flip-flop A35-2 which controls switch A1-1. Switch A1-1 switches resistor R3 in or out of the A7-5 timing circuit and

thereby increases or shortens the one-shot delay by one quarter horizontal line. If over a period of time, the time out of A7-5 should drift close to the arrival of an H-pulse, flip-flop A35-2 is toggled again.

4-12. Character Storage and Retrieval

During the first few lines of each frame, incoming data is stored in RAM A12. After the vertical position one-shot times out, the time data stored in RAM A12 is read out and becomes the address (partial) of the numeral it represents which is stored in ROM A18. Data storage RAM A12 is a 4-bit-by-16-word memory. Only 8 words are used for storing time data; the remaining 8 words are unused. The source of the data is identified by the logic levels on PWA connector pins 71, 73, and 75 and comes from either tape timer 1 or tape timer 2 on the Tape Timer PWA or is the time-code data from the Time-Code Reader/Generator (TCR/G). The 8 numerals that comprise a time display are stored in BCD format in 8 separate RAM locations. Data from the two tape timers and the TCR/G are continuously received on the Character Generator PWA display data input lines (PWA connector pins 34, 36, 31, and 29). The display address input lines (PWA connector pins 44, 42, and 40) are continuously cycling through a three-bit binary count (0–7) at a rate of 250 kHz. The TCR/G clock, which appears at PWA input pin 46, is cycling at the same rate.

Writing into RAM A12 is enabled by the inverted and buffered output of AND gate A41-3. The vertical position output of one-shot A7-5, which goes high at field rate, is applied to A41-2. When the 3 bits of display address (pins 44, 42, 40) have stabilized on the RAM address inputs (A0, A1, A2) and when the 4 bits of display data have settled on the RAM data inputs (D0, D1, D2, D3), the next clock pulse (pin 46) fires one-shot A5-13. The one-shot output completes AND gate A41-4, and the gate output writes the display data into the selected RAM address. The chip select for A12 is provided through NOR gate A9-10 by the vertical position output of A7-5. This action is repeated until 8 of the RAM addresses have been loaded.

Following loading of the numbers into the RAM during the first few lines of a field, nothing else happens until the vertical position one-shot times out. After the one-shot has timed out, under control of the write/read logic, the data storage RAM A12 is enabled for readout. During readout, multiplexer A19 channels the data on lines B_0–B_3 to the address lines of the data storage RAM. Counter A26 provides the addresses to the B_0-B_3 lines of the multiplexer.

Counter A26 is a 4-bit down counter that is clocked through eight states during the course of the scan of horizontal slices of the tape time display on the screen. The counter is initialized when highs are parallel-loaded into its four cells by the frame rate pulse generated by gate A39-10. The count is decremented by pulses produced by gate A8-10. The timing and control circuit generates pulses that are applied to input 9 of NAND gate A8. A pulse occurs prior to the scan of each character position. These pulses are selectively enabled by pulses produced by PROM A23. PROM A23 enables A8-10 only during display character positions that require tape time data from RAM A12 — namely character positions 4 and 5, 7 and 8, 10 and 11, 13 and 14 (see Figure 4-3). In this way counter A26 is decremented (and the next data storage RAM memory location is addressed) only when a character position of the display that presents time data is about to be scanned.

Table 4-2 indicates that PROM A23 data output line DO_1 is high when and only when the character position counter A31 is at character position counts 4 and 5, 7 and 8, 10 and 11, 13 and 14. The DO_1 line of PROM A23 is used expressly for decrementing counter A26.

4-13. Timing and Control

Data flows through the Character Generator PWA at a rate that requires a pipelining technique. That is, display data and display address for a specific character are written into RAM A21 while the 7 horizontal slices of the preceding character are being clocked through shift registers A4 and A25 to the output. The output of the oscillator, composed of A3 and associated components, appears at A38-10. This is the undelayed clock which drives timing and control circuit A21. The undelayed clock is applied to L1 and C37, which delay the clock to compensate for propagation delays

in A21. Delayed clock appears at A38-12 and advances the character position counter A31 when clock input to the counter is enabled. Delayed clock also appears at A28-10 to shift the character data shift register A4 and at A28-12 to shift the border data shift register A25.

Timing and control circuit A21 is a 4-bit bidirectional shift register connected as a Johnson counter which shifts right and counts through 7 states, T1 through T7, as shown in Figure 4-8. The 7 states correspond to the 7 columns of elements in each character. The gates and inverters associated with the Q1–Q4 outputs of A21 detect five discrete states of A21 output to drive the rest of the logic in an orderly, synchronous manner.

The inverted and buffered output of AND gate A8-4 turns on switch A17 during time frame T2, T3, T4 to gate 3 bits of the address word from A16 and 3 bits of the address word from A23 to ROM A18. The remaining 4 bits of the address word are supplied by RAM A21. After the address lines have settled at the ROM inputs, gate A43-9 goes high during T3 and strobes the address word into the ROM. Inverter A28-6 goes low during time frame T5, T6, T7 enabling the output of the ROM to the data bus to shift registers A4 and A25. This is the OEL input. The OEH input is held high by the output of OR gate A14-6 during the 7 slice counts of A16. AND gate A29-3 goes high during time T6, enabling the character position counter A31 to be advanced by the next delayed clock pulse. Thus, this counter is advanced only once for each 7 clock pulses. The output of AND gate A29-11 goes high during T7, parallel-loading the ROM output word into shift registers A4 and A25. The shift registers are shifted by the undelayed clock to the video out line.

Before data addressed in ROM A18 is place on the bus, the next address is being formed. The high produced at A8-4 during T2, AND-gated with A23-12, increments counter A26 and thereby places new address bits on the output lines of RAM A12.

4-14. Power Supplies

The VPR-2 main power supply furnishes +12V, –12V, and +5V to the Character Generator PWA. A +10V supply is developed on the PWA. Voltage regulator A6 and VR1 drop the +12V supply to +10V. The +10V is used for the digital logic because some of the integrated circuits have an absolute maximum rating of +11V.

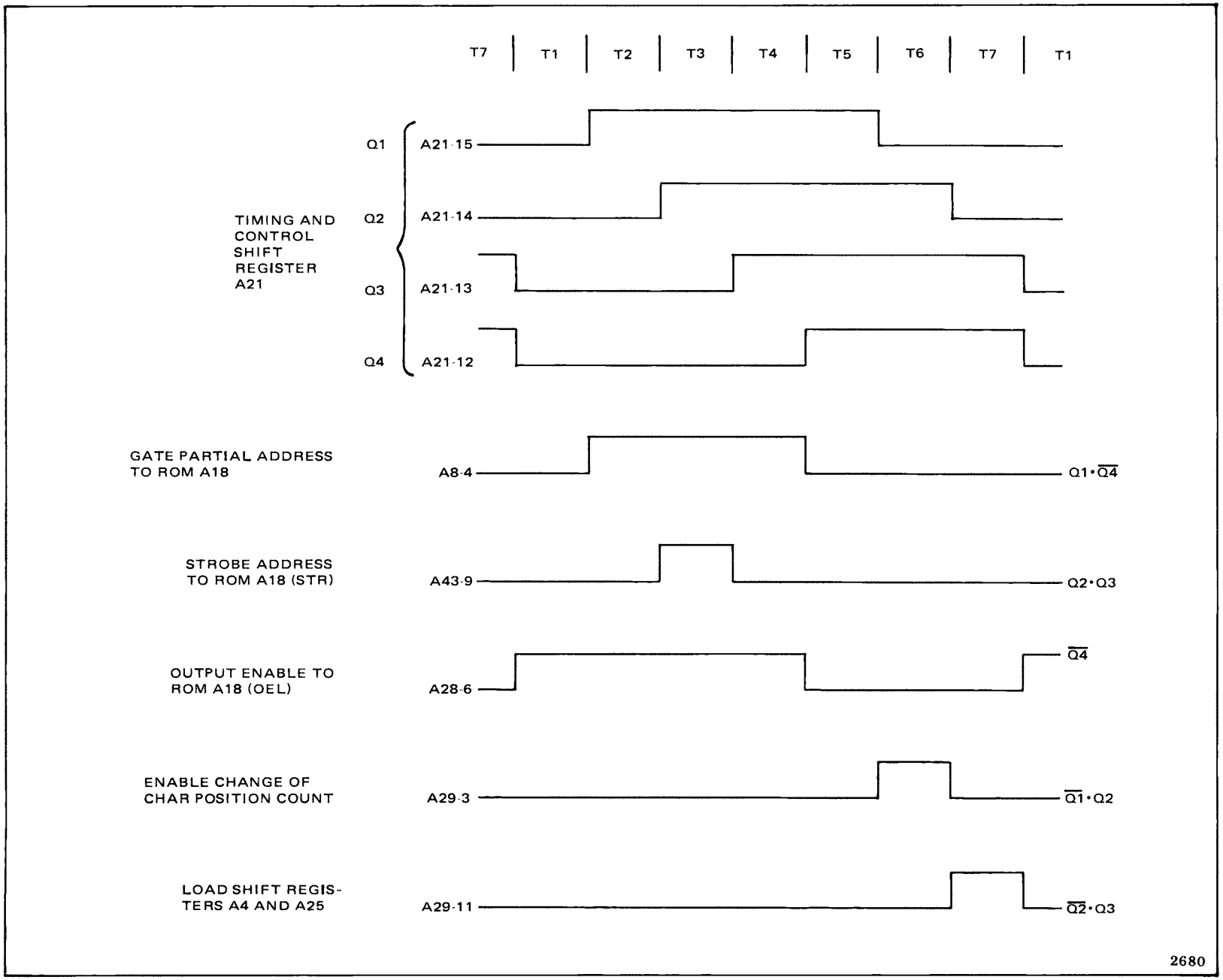

Figure 4-8. Timing and Control Timing Diagram

SECTION 5
MAINTENANCE

5-1. INTRODUCTION

This section provides maintenance information for the Character Generator PWA. The Character Generator PWA requires no scheduled maintenance. Following replacement of component parts realignment may be necessary.

5-2. MAINTENANCE PRECAUTIONS

All MOS/CMOS devices are susceptible to damage by the presence of electrostatic fields in the gate oxide region of the device. The gate oxide thickness of these devices is nominally 1200 A° (120 nm) which limits the maximum voltage which can be applied to any input of a device to 60V with a reasonable safety factor. Since the gate capacitance is typically 10 pf, a static charge of 600 X 10^{-12} coulombs will produce a gate voltage of 60V (using the formula Q = CV). Therefore, random generation of any electrostatic charges must be avoided.

Almost all MOS/CMOS devices have input protection networks which are effective in a large number of device-handling situations. They are not effective in all cases. To make them so would obviously affect performance of the devices. Therefore, the following suggestions are made to assure proper techniques and procedures for handling MOS and CMOS integrated circuits and MOSFET transistors during test operations. Proper handling will eliminate degradation of performance or destruction of these parts due to static electrical charge.

1. All electrical equipment should be hard-wired to ground. Soldering iron tips, metal parts of fixtures, and tools and handling systems should be grounded.
2. Soldering irons, solder pots, or flow soldering equipment should be grounded whenever in contact with printed wiring boards and/or MOS devices.
3. Ungrounded automatic insertion equipment or other handling equipment that precludes the use of suitable device lead grounding techniques during incoming inspection or handling should be avoided.
4. All work stations should have conductive work surfaces and conductive material floor mats connected to a common ground system. Chairs and stools should be made of metal or covered with antistatic material.
5. Technicians should wear antistatic smocks and gloves (cotton preferably).
6. All leads of MOS devices should be kept shorted until insertion in the printed wiring board. Conductive foam, dummy connectors, metal tubes, antistatic tubes, and foil lined containers are all suitable.
7. MOS devices and/or circuit boards containing MOS devices should not be inserted into or removed from test circuits with power on because transient voltages may cause permanent damage.
8. When printed wiring boards containing mounted MOS devices are removed from equipment for test, shipping, storage, etc., "dummy" connectors should be used to electrically short all printed wiring board terminals together. A suitable alternative would be to contain the board in antistatic material. These precautions should be taken until the subassembly is inserted into the complete system in which the proper voltages are applied.

9. Subassembled modules and printed wiring boards should be manufactured and handled using the above suggestions for individual MOS devices. Subassemblies should not be fixtured, stored, or transported in polystyrene or other high dielectric materials.

5-3. ALIGNMENT

Realign the Character Generator PWA as follows:

CAUTION

WHENEVER THE CHARACTER GENERATOR PWA IS REMOVED OR REPLACED IN THE VPR-2, ENSURE THAT VPR-2 MAIN POWER HAS FIRST BEEN TURNED OFF.

1. With the VPR-2 main power turned off, remove the Character Generator PWA from the VPR-2; place the PWA on an extender and insert the extender in slot 7 of the VPR-2.
2. Turn on the VPR-2 main power and initiate the play mode.
3. Set the BORD/WINDOW toggle switch on the Character Generator PWA to BORD.
4. Set the CHAR SIZE rotary switch to 4 to select the largest characters.
5. Observe the monitor and adjust potentiometer R34 (see Figure 5-1) to center the characters within their borders. Then rotate the CHAR SIZE switch to 1 and check small size display for centering.
6. Adjust inductor L3 to center the display between the left and right sides of the screen.
7. Turn off VPR-2 main power.
8. Remove the extender board and replace Character Generator PWA back into slot 7 of the VPR-2.

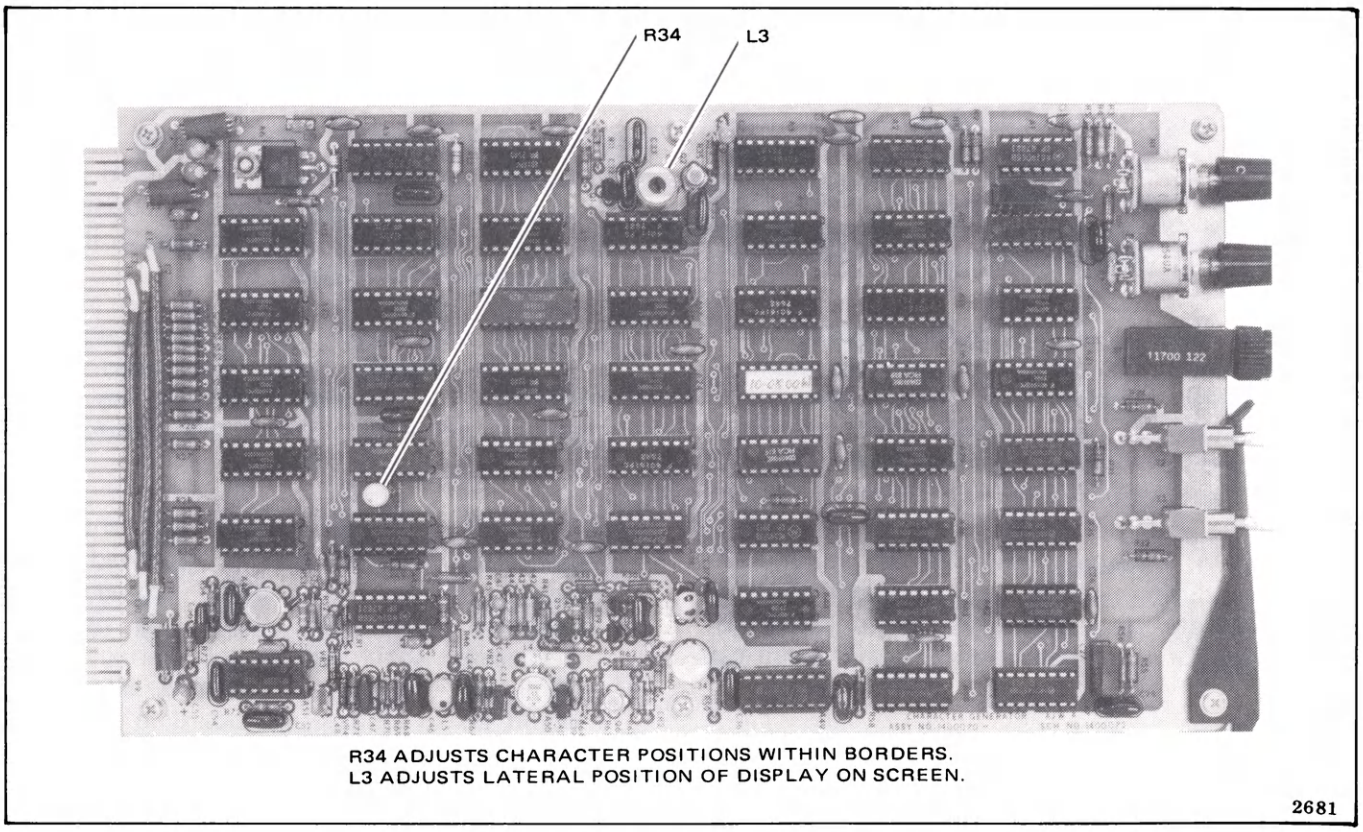

Figure 5-1. Character Generator PWA Adjustments

SECTION 6

PARTS LISTS AND SCHEMATICS

This section of the manual provides the parts list, assembly drawing and schematic diagram for the VPR-2 Character Generator, Ampex Part No. 1400073-01.

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Integrated Circuits	—	A-1

1400073-01 VPR-2 CHARACTER GENERATOR PWA, NO. 7 REV. –
NEXT HIGHER ASSEMBLY CATALOG

ITEM NO.	PART NUMBER	DESCRIPTION	REF DESIG	QTY REQD PER DASH NUMBER -01
1				
2				
3	1400075	SCHEMATIC	(-)	
4	1400261-02	KNOB, MACHINED	REF: S1	1
5	1400003-01	SHIELD		1
6	1400004-01	HANDLE		1
7	1400005-AW	LABEL		1
8	1377230	PROM 63S141	A18	-01
9	1400310	PROM 74S287	A23	-01
10	051-770	INDUCTOR FILTER	FL1-3	3
11	013-358	DIODE, ZENER, 5.1V (1N751A)	VR1	1
12	013-172	DIODE, ZENER, 4.3V (1N749A)	VR3,4	2
13	013-983	DIODE, ZENER, 5.6V (1N752A)	VR2	1
14	013-599	DIODE, SIGNAL (1N4531)	CR1,2	2
15	580-453	TRANSISTOR, (2N5639)	Q1	1
16	014-506	TRANSISTOR, (2N2501)	Q2,6,7	3
17	014-780	TRANSISTOR (MPS6514)	Q3,4,5	3
18	075-274	WIRING BOARD	REF: R1,2	2
19	075-273	MTG. PLATE	REF: R1,2	2
20				
21	064-116	CAPACITOR, CER., .1uF, 50V	C3,5,6,8,9,11,15-22,24-26,29,31,39,50,56	22
22	030-963	CER., .1uF, 100V 10%	C40,43	2
23	034-199	MICA, 300pF, 500V, ±5%	C52	1
24	064-314	MONO., 1.0uF, 50V, 20%	C48,51	2
25	064-062	MONO., .1uF, 100V	C12,45,58,49	4
26	056-697	MICA, 7pF 500V, ±.5pF	C33	1
27	034-532	MICA, 1pF, 500V, ±.5pF	C47	1
28	034-156	5pF, 500V, ±.5pF	C35	1
29	034-215	10pF, 500V, ±.5pF	C37	1
30	034-945	12pF, 500V, ±5%	C54	1
31	034-177	100pF, 500V, 5%	C23,57	2
32	034-688	30pF, ±.5pF, 500V	C10,53	2
33	034-962	33pF, 500V, 5%	C32	1
34	034-937	160pF, 500V, 5%	C38	1
35	034-919	270pF, 500V, 1%	C2	1
36	034-241	360pF, 500V, 1%	C28,30	2
37	056-216	CAPACITOR, MICA, 500pF, 500V, 1%	C36	1

AMPEX | Ampex Corporation REDWOOD CITY, CALIFORNIA	CODE IDENT NO. 92739	LIST OF MATERIALS	LM-1400073 SHEET 2 OF 4	REV —

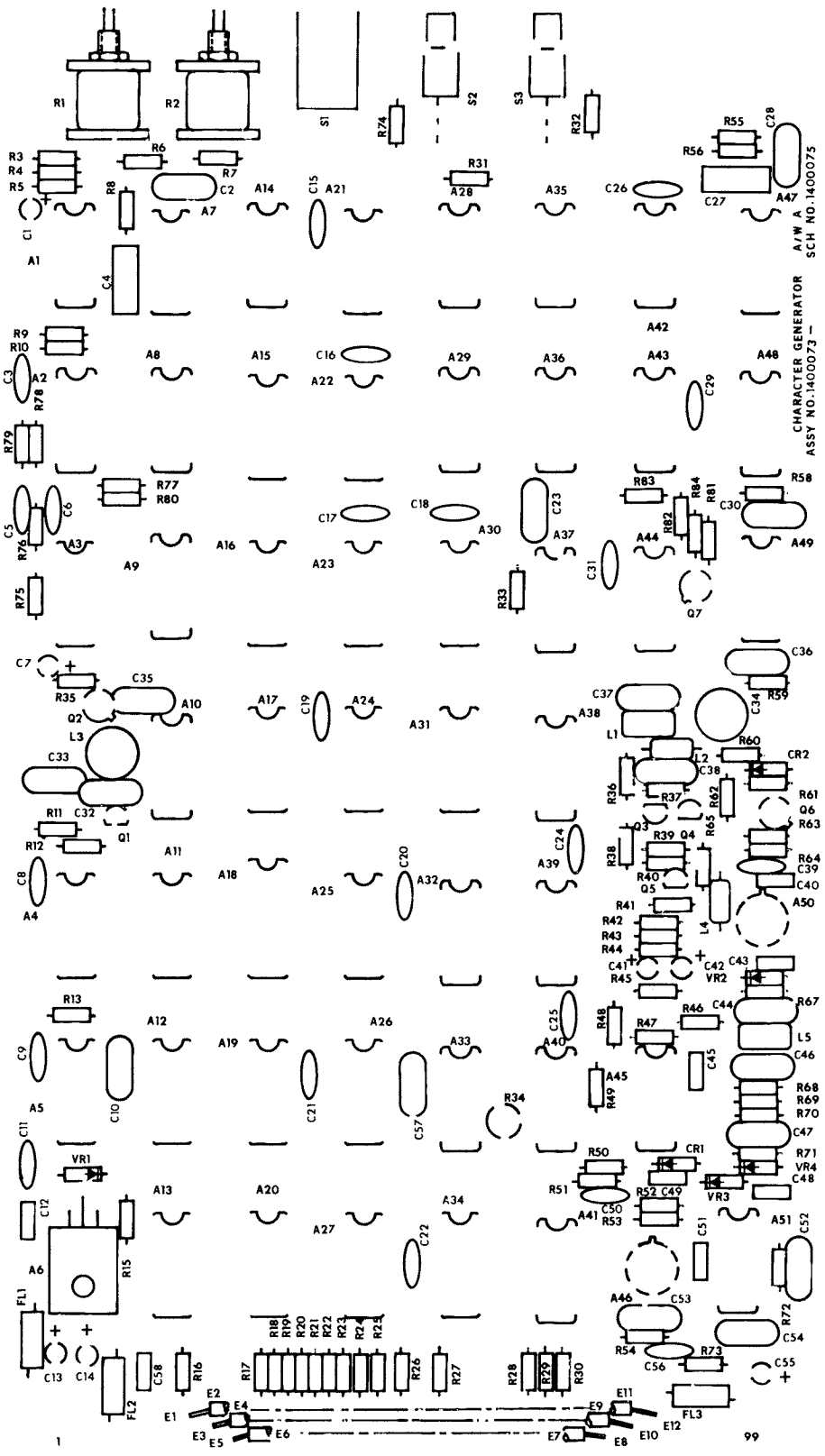
ITEM NO.	PART NUMBER	DESCRIPTION	REF DESIG	QTY REQD PER DASH NUMBER -01
38	034-320	CAPACITOR, MICA, 750pF, 300V, 5%	C44,46	2
39				
40	038-254	CAPACITOR, VAR, 9-35pF, 100V	C34	1
41	035-893	CAPACITOR, MYLAR., .1uF, 50V, 5%	C4,27	2
42	037-954	CAPACITOR, TANT, 22uF, 15V	C1,7,13,14,55	5
43	037-962	CAPACITOR, TANT, 4.7uF, 10V	C41,42	2
44				
45	066-677	RESISTOR, C.F., 68 OHM, 1/4W, 5%	R54	1
46	066-826	2K OHM,	R49,50,71	3
47	066-824	1.5K OHM	R39,41,61	3
48	066-938	47 OHM	R37,40,73	3
49	066-859	240 OHM	R72	1
50	066-818	470 OHM	R47, 84	2
51	066-839	560 OHM	R15	1
52	066-840	680 OHM	R65	1
53	066-820	750 OHM	R67,68	2
54	066-663	220 OHM	R46	1
55	066-668	4.7K OHM	R16-30	15
56	066-665	1K OHM	R33,60,62,75-83	12
57	066-689	2.2K OHM	R35,52	2
58	066-830	10K OHM	R9,10,31,32,74	5
59	066-873	20K OHM	R11,12	2
60	066-652	470K OHM	R53	1
61	066-829	6.8K OHM	R51	1
62	076-050	270K OHM	R4	1
63	066-958	C.F., 75K OHM 1/4W, 5%	R5	1
64	062-864	M.F., 150 OHM 1/8W, 1%	R64	1
65	062-885	309 OHM	R3	1
66	062-642	6.81K OHM	R48	1
67	066-442	10.5K OHM	R8	1
68	066-925	22.1K OHM	R56	1
69	066-802	9.76K OHM	R58	1
70	062-983	10K OHM	R13,55	2
71	066-752	11.8K OHM	R63	1
72	062-601	100K OHM	R42,44,59	3
73	066-193	2.15K OHM	R70	1
74	076-384	806K OHM	R7	1
75	062-943	2.32K OHM	R69	1
76	062-935	1.65K OHM	R38	1
77	062-624	1K OHM	R36	1
78	062-988	13.7K OHM	R6	1
79				
80	062-945	2.43K OHM	R43	1
81	062-950	RESISTOR, M.F., 2.74K OHM 1/8W, 1%	R45	1
82				

AMPEX | Ampex Corporation Redwood City, California	CODE IDENT NO 92739	LIST OF MATERIALS	LM-1400073 SHEET 3 OF 4	REV —

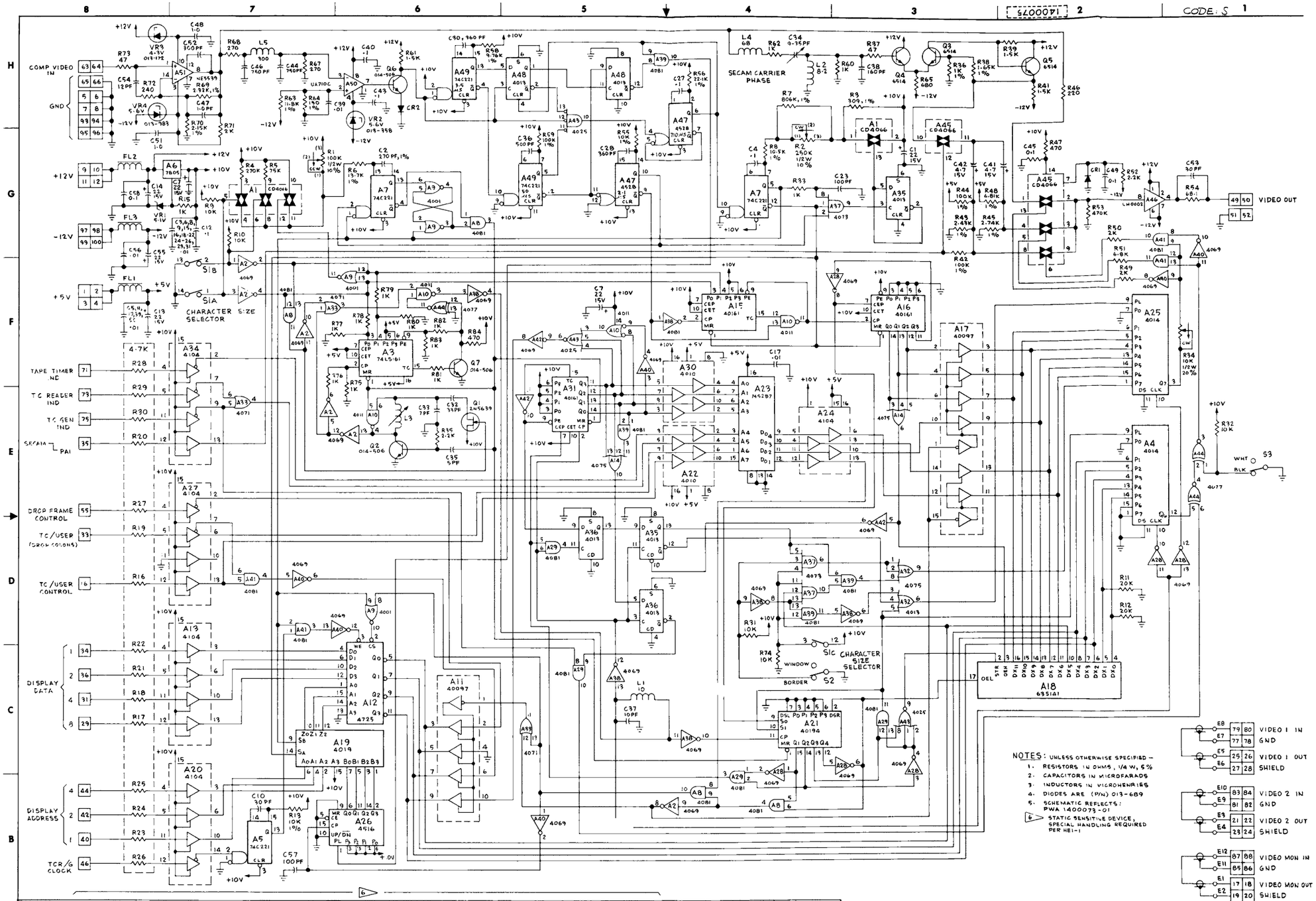
ITEM NO	PART NUMBER	DESCRIPTION	REF DESIG	QTY REQD PER DASH NUMBER -01
83	058-611	RESISTOR, VAR., 10K OHM, 1/2W, 20%	R34	1
84	058-809	RESISTOR, VAR., 100K OHM, 1/2W, 10%	R1	1
85	075-164	RESISTOR, VAR., 250K OHM, 1/2W, 10%	R2	1
86				
87	068-064	INDUCTOR, FIXED, 300uH, 5%	L5	1
88	051-870	INDUCTOR, FIXED, 10uH, 5%	L1	1
89	540-017	INDUCTOR, FIXED, 68uH	L4	1
90	540-028	INDUCTOR, FIXED, 8.2uH	L2	1
91	541-070	INDUCTOR, VAR., 22uH, ±20%	L3	1
92	119-724	SWITCH,TOGGLE, SPDT	S2,3	2
93	122-494	SWITCH, DIP, ROTARY, 6P6POS	S1	1
94				
95	586-124	INTEGRATED CIRCUIT, UA710HC	A50	1
96	586-315	LH0002CH	A46	1
97	589-973	NE5539N	A51	1
98	589-298	F4001PC	A9	1
99	587-772	74LS161	A3	1
100	587-909	F4011PC	A10	1
101	589-315	F4013PC	A35,36,48	3
102	589-299	F4014PC	A4,25	2
103	587-990	F4C19PC	A19	1
104	589-300	F4025PC	A43	1
105	589-301	F4069PC	A2,28,38,40,42	5
106	589-302	F4071PC	A33	1
107	589-303	F4073PC	A37	1
108	589-304	F4075PC	A14,32	2
109	589-305	F4077PC	A44	1
110	589-306	F4081PC	A8,29,39,41	4
111	589-307	F4104PC	A13,20,24,27,34	5
112	589-308	F4516PC	A26	1
113	589-309	F4528PC	A47	1
114	589-310	F4725PC	A12	1
115	589-311	F40097PC	A11,17	2
116	589-312	F40161PC	A15,16,31	3
117	589-313	F40194PC	A21	1
118	587-680	CD4066AE	A1,45	2
119	589-019	74C221	A5,7,49	3
120	587-959	CD4010BE	A22,30	2
121	587-438	INTEGRATED CIRCUIT, 7805CT	A6	1
122	582-134	SOCKET, 16 PIN	REF: A26	1
123	582-161	SOCKET, 18 PIN	REF: A18	1
124	249-144	KNOB	REF: R1,2	2
125				
126	280-130	SPACER, TRANSISTOR TO-18		2
127	283-105	SPACER, PLAIN, .140 ID, .125 LG		1

AMPEX | Ampex Corporation REDWOOD CITY, CALIFORNIA	CODE IDENT NO 92739	LIST OF MATERIALS	LM-1400073 SHEET 4 OF 4	REV —

ITEM NO.	PART NUMBER	DESCRIPTION	REF DESIG	QTY REQD PER DASH NUMBER -01
128				
129	473-325	SCREW,MACH,PAN HD, XREC, 4-40 X .312 LG.		6
130	471-063	SCREW, MACH,PAN HD,xrec, 4-40 X .438 LG.		1
131	501-169	WASHER, SMALL PATTERN #4		6
132	502-002	WASHER, LOCK #4		2
133	506-011	WASHER, BOWED		1
134	616-569	COAX CABLE, 75 OHMS		A/R
135				
136				
137				
138				
139	493-005	NUT, LOCKING, HEX, 4-40		1
140				
141	477-516	SCREW,SET, 4-40 X .188 LG.	REF: S1	1
		3 STATIC SENSITIVE SPECIAL HANDLING REQUIRED		



Assembly No. 1400073. VPR-2 Character Generator PWA, No. 7



NOTES: UNLESS OTHERWISE SPECIFIED —
1. RESISTORS 1W OHMS, 1/4 W, 5%
2. CAPACITORS IN MICROFARADS
3. INDUCTORS IN MICROHENRIES
4. DIODES ARE (P/N) 013-689
5. SCHEMATIC REFLECTS: PWA 1400073-01
6. STATIC SENSITIVE DEVICE, SPECIAL HANDLING REQUIRED PER HEI-1

I. C. LIST

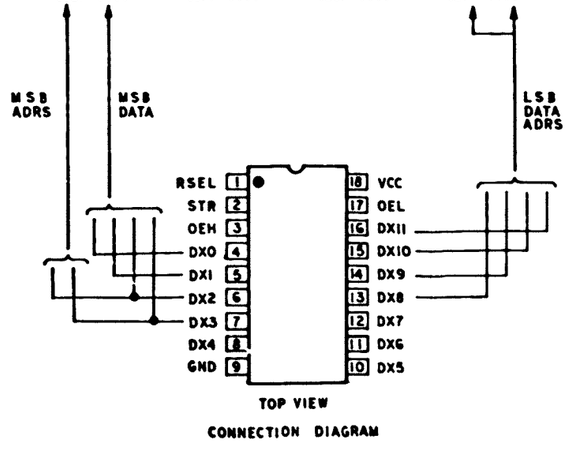
REF DESIG	A50	A51	A10	A4,25	A43	A33	A14,32	A8,29,39,41	A26	A12	A15,16,31	A1,45	A22,30	A18
AMPEX P/N	586-124	589-773	587-909	589-299	589-300	589-302	589-304	589-306	589-308	589-310	589-312	587-680	587-959	1377230
VENDOR P/N	UH710HC	NE5539N	F4011PC	F4014PC	F4025PC	F4071PC	F4075PC	F4081PC	F4516PC	F4725PC	F40161PC	CD4066AE	4010	6S5141
VOLTAGE PIN	+12(8),-12(4)	—	+10(14)	+10(16)	+10(14)	+10(14)	+10(14)	+10(14)	+10(16)	+10(16)	+10(16)	+10(16)	+10(16),+5(1)	—
GROUND PIN	1	7	7	8	7	7	7	7	8	8	8	8	8	—
REF DESIG	A46	A9	A35,36,48	A19	A2,28,38,40;42	A37	A44	A13,20,24,27,34	A47	A11,17	A21	A5,7,49	A6	A23
AMPEX P/N	586-315	589-298	589-315	589-990	589-301	589-303	589-305	589-307	589-309	589-311	589-313	589-019	587-438	1400310
VENDOR P/N	LH0002CH	F4001PC	F4019PC	F4019PC	F4069PC	F4073PC	F4077PC	F4104PC	F4528PC	F40097PC	F40194PC	74C221	7805CT	74S287
VOLTAGE PIN	+12(1,8),-12(7,8)	+10(14)	+10(14)	+10(16)	+10(14)	+10(14)	+10(14)	+10(1),-10(16)	+10(16)	+10(16)	+10(16)	+10(16)	+10(14)	+5(16)
GROUND PIN	—	7	7	8	7	7	7	8	8	8	8	8	7	8

FIELD SERVICE SUBST LIST	
AMPEX P/N	NEAREST COMM EQUIV
013-358	1N751A
013-689	FD6016
013-983	1N752A
014-267	2N2219
014-506	2N2501
580-453	2N5639
A3	74LS161
587-772	
+5(16)	
8	

REF DESIG	
LAST USED	NOT USED
A51	R14,57
C58	
CR2	
E12	
FL3	
L5	
Q7	
R84	
S3	
VR4	

Schematic No. 1400075—.
Character Generator

HEX ADRS	HEX DATA																			
0000	0000	0040	0000	0080	0000	00C0	0000	0100	0000	0140	0000	0180	0000	01C0	0000	0200	0000	0240	0000	0280	0000	02C0	0000	0300	0000	0340	0000	0380	0000	03C0	0010
0001	0000	0041	0000	0081	0000	00C1	0000	0101	0000	0141	0000	0181	0000	01C1	0000	0201	0000	0241	0000	0281	0000	02C1	0000	0301	0000	0341	0000	0381	0000	03C1	0000
0002	0000	0042	0000	0082	0000	00C2	0000	0102	0000	0142	0000	0182	0000	01C2	0000	0202	0000	0242	0000	0282	0000	02C2	0000	0302	0000	0342	0000	0382	0000	03C2	0000
0003	0000	0043	0000	0083	0000	00C3	0000	0103	0000	0143	0000	0183	0000	01C3	0000	0203	0000	0243	0000	0283	0000	02C3	0000	0303	0000	0343	0000	0383	0000	03C3	0000
0004	0000	0044	0000	0084	0000	00C4	0000	0104	0000	0144	0000	0184	0000	01C4	0000	0204	0000	0244	0000	0284	0000	02C4	0000	0304	0000	0344	0000	0384	0000	03C4	0000
0005	0000	0045	0000	0085	0000	00C5	0000	0105	0000	0145	0000	0185	0000	01C5	0000	0205	0000	0245	0000	0285	0000	02C5	0000	0305	0000	0345	0000	0385	0000	03C5	0000
0006	0000	0046	0000	0086	0000	00C6	0000	0106	0000	0146	0000	0186	0000	01C6	0000	0206	0000	0246	0000	0286	0000	02C6	0000	0306	0000	0346	0000	0386	0000	03C6	0000
0007	0000	0047	0000	0087	0000	00C7	0000	0107	0000	0147	0000	0187	0000	01C7	0000	0207	0000	0247	0000	0287	0000	02C7	0000	0307	0000	0347	0000	0387	0000	03C7	0000
0008	0000	0048	0000	0088	0000	00C8	0000	0108	0000	0148	0000	0188	0000	01C8	0000	0208	0000	0248	0000	0288	0000	02C8	0000	0308	0000	0348	0000	0388	0000	03C8	0000
0009	007F	0049	007F	0089	007F	00C9	007F	0109	007F	0149	007F	0189	007F	01C9	007F	0209	007F	0249	007F	0289	007F	02C9	007F	0309	007F	0349	007F	0389	007F	03C9	007F
000A	0FFF	004A	0FFF	008A	0FFF	00CA	0FFF	010A	0FFF	014A	0FFF	018A	0FFF	01CA	0FFF	020A	0FFF	024A	0FFF	028A	0FFF	02CA	0FFF	030A	0FFF	034A	0FFF	038A	0FFF	03CA	0FFF
000B	027F	004B	027F	008B	027F	00CB	027F	010B	027F	014B	027F	018B	027F	01CB	027F	020B	027F	024B	027F	028B	027F	02CB	027F	030B	027F	034B	027F	038B	027F	03CB	027F
000C	021C	004C	021C	008C	021C	00CC	021C	010C	021C	014C	021C	018C	021C	01CC	021C	020C	021C	024C	021C	028C	021C	02CC	021C	030C	021C	034C	021C	038C	021C	03CC	021C
000D	021C	004D	021C	008D	021C	00CD	021C	010D	021C	014D	021C	018D	021C	01CD	021C	020D	021C	024D	021C	028D	021C	02CD	021C	030D	021C	034D	021C	038D	021C	03CD	021C
000E	021C	004E	021C	008E	021C	00CE	021C	010E	021C	014E	021C	018E	021C	01CE	021C	020E	021C	024E	021C	028E	021C	02CE	021C	030E	021C	034E	021C	038E	021C	03CE	021C
000F	001C	004F	001C	008F	001C	00CF	001C	010F	001C	014F	001C	018F	001C	01CF	001C	020F	001C	024F	001C	028F	001C	02CF	001C	030F	001C	034F	001C	038F	001C	03CF	001C
0010	0000	0050	0000	0090	0000	00D0	0000	0110	0000	0150	0000	0190	0000	01D0	0000	0210	0000	0250	0000	0290	0000	02D0	0000	0310	0000	0350	0000	0390	0000	03D0	0000
0011	000E	0051	000E	0091	000E	00D1	000E	0111	003F	0151	003F	0191	003F	01D1	003F	0211	003F	0251	003F	0291	003F	02D1	003F	0311	003F	0351	003F	0391	003F	03D1	003F
0012	011E	0052	011E	0092	011E	00D2	011E	0112	07BF	0152	07BF	0192	07BF	01D2	07BF	0212	07BF	0252	07BF	0292	07BF	02D2	07BF	0312	07BF	0352	07BF	0392	07BF	03D2	07BF
0013	031E	0053	031E	0093	031E	00D3	031E	0113	00BF	0153	00BF	0193	00BF	01D3	00BF	0213	043F	0253	043F	0293	043F	02D3	043F	0313	043F	0353	043F	0393	043F	03D3	043F
0014	011E	0054	011E	0094	011E	00D4	011E	0114	07BF	0154	07BF	0194	07BF	01D4	07BF	0214	0438	0254	0438	0294	0438	02D4	0438	0314	0438	0354	0438	0394	0438	03D4	0438
0015	011F	0055	011F	0095	011F	00D5	011F	0115	043F	0155	043F	0195	043F	01D5	043F	0215	043F	0255	043F	0295	043F	02D5	043F	0315	043F	0355	043F	0395	043F	03D5	043F
0016	039F	0056	039F	0096	039F	00D6	039F	0116	07BF	0156	07BF	0196	07BF	01D6	07BF	0216	07BF	0256	07BF	0296	07BF	02D6	07BF	0316	07BF	0356	07BF	0396	07BF	03D6	07BF
0017	001F	0057	001F	0097	001F	00D7	001F	0117	003F	0157	003F	0197	003F	01D7	003F	0217	003F	0257	003F	0297	003F	02D7	003F	0317	003F	0357	003F	0397	003F	03D7	003F
0018	0000	0058	0000	0098	0000	00D8	0000	0118	0000	0158	0000	0198	0000	01D8	0000	0218	0000	0258	0000	0298	0000	02D8	0000	0318	0000	0358	0000	0398	0000	03D8	0000
0019	0000	0059	0000	0099	0000	00D9	0000	0119	0000	0159	0000	0199	0000	01D9	0000	0219	0000	0259	0000	0299	0000	02D9	0000	0319	0000	0359	0000	0399	0000	03D9	0000
001A	001C	005A	001C	009A	0000	00DA	0000	011A	001C	015A	001C	019A	0000	01DA	0000	021A	001C	025A	000E	029A	001C	02DA	000E	031A	001C	035A	090C	039A	001C	03DA	000E
001B	021C	005B	021C	009B	0000	00DB	0000	011B	021C	015B	021C	019B	0000	01DB	0000	021B	021C	025B	010E	029B	021C	02DB	010E	031B	021C	035B	010E	039B	021C	03DB	010E
001C	001C	005C	001C	009C	0000	00DC	0000	011C	001C	015C	001C	019C	0000	01DC	0000	021C	001C	025C	000E	029C	001C	02DC	000E	031C	001C	035C	000E	039C	001C	03DC	000E
001D	021C	005D	021C	009D	0000	00DD	0000	011D	021C	015D	021C	019D	0000	01DD	0000	021D	021C	025D	011E	029D	021C	02DD	011E	031D	021C	035D	011E	039D	021C	03DD	011E
001E	001C	005E	001C	009E	0000	00DE	0030	011E	001C	015E	001C	019E	0000	01DE	0000	021E	001C	025E	021E	029E	001C	02DE	021E	031E	001C	035E	021E	039E	001C	03DE	021E
001F	0000	005F	0000	009F	0000	00DF	0800	011F	0000	015F	0000	019F	0000	01DF	0000	021F	0000	025F	001C	029F	0000	02DF	001C	031F	0000	035F	001C	039F	0000	03DF	001C
0020	0000	0060	0000	00A0	0000	00E0	0000	0120	0000	0160	0000	01A0	0C00	01E0	0000	0220	0000	0260	0000	02A0	0000	02E0	0000	0320	0000	0360	0000	03A0	0000	03E0	0000
0021	0000	0061	0000	00A1	0000	00E1	0000	0121	0600	0161	0000	01A1	0000	01E1	0000	0221	0000	0261	0000	02A1	0000	02E1	0000	0321	0000	0361	0060	03A1	0000	03E1	0000
0022	0000	0062	0000	00A2	0000	00E2	0000	0122	0000	0162	0000	01A2	0000	01E2	0000	0222	0000	0262	0000	02A2	0000	02E2	0000	0322	0000	0362	0000	03A2	0000	03E2	0000
0023	007F	0063	007F	00A3	007F	00E3	007F	0123	007F	0163	007F	01A3	C07F	01E3	007F	0223	007F	0263	007F	02A3	007F	02E3	007F	0323	007F	0363	007F	03A3	007F	03E3	007F
0024	0FFF	0064	0FFF	00A4	0FFF	00E4	0FFF	0124	0FFF	0164	0FFF	01A4	0FFF	01E4	0FFF	0224	0FFF	0264	0FFF	02A4	0FFF	02E4	0FFF	0324	0FFF	0364	0FFF	03A4	0FFF	03E4	0FFF
0025	007F	0065	007F	00A5	007F	00E5	007F	0125	007F	0165	007F	01A5	007F	01E5	007F	0225	007F	0265	007F	02A5	007F	02E5	007F	0325	007F	0365	007F	03A5	007F	03E5	007F
0026	0000	0066	0000	00A6	0000	00E6	0000	0126	0000	0166	0000	01A6	0000	01E6	0000	0226	0000	0266	0000	02A6	0000	02E6	0000	0326	0000	0366	0000	03A6	0000	03E6	0000
0027	0000	0067	0000	00A7	0000	00E7	0000	0127	0600	0167	0000	01A7	0000	01E7	0000	0227	0000	0267	0000	02A7	0000	02E7	0000	0327	0000	0367	0000	03A7	0000	03E7	0000
0028	0000	0068	0000	00A8	0000	00E8	0300	0128	0000	0168	0000	01A8	0000	01E8	0000	0228	0000	0268	0000	02A8	0000	02E8	0000	0328	0000	0368	0000	03A8	0000	03E8	0000
0029	0000	0069	0000	00A9	0000	00E9	0000	0129	0000	0169	0000	01A9	0000	01E9	0000	0229	0000	0269	0000	02A9	0000	02E9	0000	0329	0000	0369	0000	03A9	0000	03E9	0000
002A	0000	006A	0000	00AA	0000	00EA	0000	012A	0000	016A	0000	01AA	0000	01EA	0000	022A	0000	026A	0000	02AA	0000	02EA	0000	032A	0000	036A	0000	03AA	0000	03EA	0000
002B	0000	006B	0000	00AB	0000	00EB	0000	012B	0000	016B	0000	01AB	0000	01EB	0000	022B	0000	026B	0000	02AB	0000	02EB	0000	032B	0000	036B	0000	03AB	0000	03EB	0000
002C	0000	006C	0000	00AC	0000	00EC	0000	012C	0000	016C	0000	01AC	0000	01EC	0000	022C	0000	026C	0000	02AC	0000	02EC	0000	032C	0000	036C	0000	03AC	0000	03EC	0000
002D	0000	006D	0000	00AD	0000	00ED	0000	012D	0000	016D	0000	01AD	0000	01ED	0000	022D	0000	026D	0000	02AD	0000	02ED	0000	032D	0000	036D	0000	03AD	0000	03ED	0000
002E	0000	006E	0000	00AE	0000	00EE	0000	012E	0000	016E	0000	01AE	0000	01EE	0000	022E	0000	026E	0000	02AE	0000	02EE	0000	032E	0000	036E	0000	03AE	0000	03EE	0000
002F	0000	006F	0000	00AF	0000	00EF	0000	012F	0000	016F	0000	01AF	0000	01EF	0000	022F	0000	026F	0000	02AF	0000	02EF	0000	032F	0000	036F	0000	03AF	0000	03EF	0000
0030	0000	0070	0000	00B0	0000	00F0	0000	0130	0000	0170	0000	01B0	0000	01F0	0000	0230	0000	0270	0000	02B0	0000	02F0	0000	0330	0C00	0370	0000	03B0	0000	03F0	0000
0031	003F	0071	000E	00B1	003F	00F1	003F	0131	003E	0171	003F	01B1	003E	01F1	003F	0231	003F	0271	003F	02B1	003F	02F1	007F	0331	003F	0371	007F	03B1	003F	03F1	003F
0032	07BF	0072	011E	00B2	07BF	00F2	07BF	0132	053E	0172	07BF	01B2	073E	01F2	07BF	0232	07BF	0272	07BF	02B2	07BF	02F2	0FFF	0332	07BF	0372	0FFF	03B2	07BF	03F2	07BF
0033	04BF	0073	031E	00B3	00BF	00F3	00BF	0133	053F	0173	043F	01B3	043F	01F3	00BF	0233	04BF	0273	04BF	02B3	04BF	02F3	04FF	0333	043F	0373	04FF	03B3	043F	03F3	043F
0034	04BF	0074	011E	00B4	07BF	00F4	039F	0134	07BF	0174	07BF	01B4	07BF	01F4	0087	0234	07BF	0274	07BF	02B4	07BF	02F4	07BF	0334	0438	0374	04BF	03B4	073E	03F4	073E
0035	04BF	0075	011F	00B5	043F	00F5	00BF	0135	013F	0175	005F	01B5	04BF	01F5	0087	0235	04BF	0275	00BF	02B5	04BF	02F5	04FF	0335	043F	0375	04FF	03B5	043F	03F5	043E
0036	07BF	0076	039F	00B6	07BF	00F6	07BF	0136	010E	0176	07BF	01B6	07BF	01F6	0087	0236	07BF	0276	039F	02B6	04BF	02F6	0FFF	0336	07BF	0376	0FFF	03B6	07BF	03F6	0438
0037	003F	0077	001F	00B7	003F	00F7	003F	0137	000E	0177	003F	01B7	003F	01F7	0007	0237	003F	0277	001F	02B7	003F	02F7	007F	0337	003F	0377	007F	03B7	003F	03F7	0038
0038	0000	0078	0000	00B8	0000	00F8	0000	0138	0000	0178	0000	01B8	0000	01F8	0000	0238	0000	0278	0000	02B8	0000	02F8	0000	0338	0000	0378	0000	03B8	0000	03F8	0000
0039	0000	0079	0000	00B9	0000	00F9	0000	0139	0000	0179	0000	01B9	9000	01F9	0000	0239	0000	0279	0000	02B9	0000	02F9	0000	0339	0000	0379	0000	03B9	0000	03F9	0000
003A	001C	007A	001C	00BA	001C	00FA	001C	013A	001C	017A	001C	01BA	001C	01FA	001C	023A	001C	027A	000E	02BA	001C	02FA	000E	033A	001C	037A	000E	03BA	001C	03FA	001C
003B	021C	007B	021C	00BB	021C	00FB	021C	013B	021C	017B	021C	01BB	021C	01FB	021C	023B	021C	027B	010E	02BB	021C	02FB	010E	033B	021C	037B	010E	03BB	021C	03FB	021C
003C	001C	007C	001C	00BC	001C	00FC	001C	013C	001C	017C	001C	01BC	001C	01FC	001C	023C	001C	027C	000E	02BC	001C	02FC	000E	033C	001C	037C	000E	03BC	001C	03FC	001C
003D	021C	007D	021C	00BD	021C	00FD	021C	013D	021C	017D	021C	01BD	021C	01FD	021C	023D	021C	027D	011E	02BD	021C	02FD	011E	033D	021C	037D	011E	03BD	021C	03FD	023C
003E	001C	007E	001C	00BE	001C	00FE	001C	013E	001C	017E	001C	01BE	001C	01FE	001C	023E	001C	027E	021E	02BE	001C	02FE	021E	033E	001C	037E	021E	03BE	001C	03FE	043C
003F	0C00	007F	0000	00BF	0000	00FF	0000	013F	0000	017F	0000	01BF	0000	01FF	0000	023F	0000	027F	001C	02BF	0000	02FF	001C	033F	0000	037F	001C	03BF	0000	03FF	0038



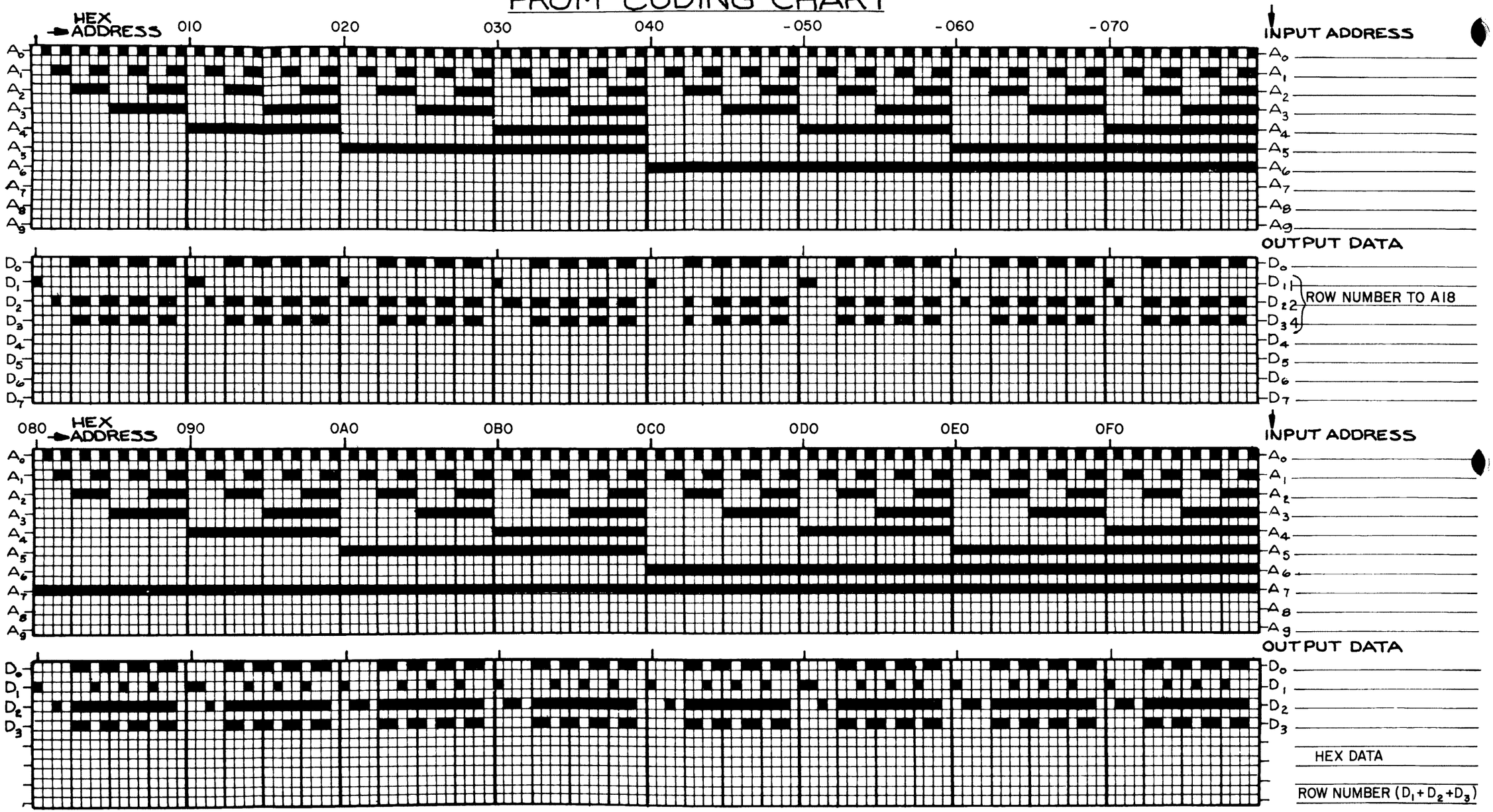
TOP VIEW

CONNECTION DIAGRAM

CMOS ROM 1024 WORD X 12 BIT. FOR PARAMETERS SEE INTERSIL IM 6312A

ROM No. 1377230.
Truth Table and Coding Chart
A18

PROM CODING CHART



PROM No. 1400310.
Status Control

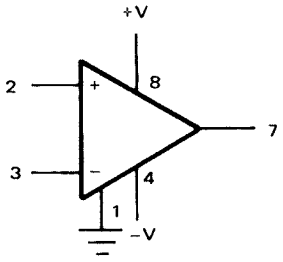
APPENDIX A

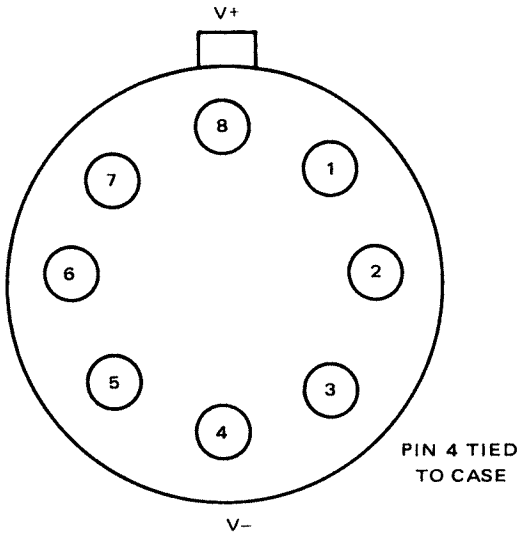
INTEGRATED CIRCUITS

Table A-1. Integrated Circuit Ampex Part Numbers

AMPEX PART NO.	MANUFACTURER'S PART NO.	MANUFACTURER	PAGE NO.
586-124	UA710HC	Fairchild	A-1
586-315	LH0002	National Semiconductor	A-1
587-319	F4011	Fairchild	A-2
587-438	7805	Fairchild	A-2
587-680	CD4066	RCA	A-3
587-905 (See 587-319)			A-2
587-959	CD4010	RCA	A-3
587-960	F4019	Fairchild	A-4
587-990 (See 587-960)			A-4
589-019	74C221	Motorola	A-4
589-298	F4001	Fairchild	A-5
589-299	F4014	Fairchild	A-5
589-300	F4025	Fairchild	A-6
589-301	F4069	Fairchild	A-6
589-302	F4071	Fairchild	A-7
589-303	F4073	Fairchild	A-7
589-304	F4075	Fairchild	A-8
589-305	F4077	Fairchild	A-8
589-306	F4081	Fairchild	A-9
589-307	F4104	Fairchild	A-9
589-308	F4516	Fairchild	A-10
589-309	F4528	Fairchild	A-10
589-310	F4725	Fairchild	A-11
589-311	F40097	Fairchild	A-11
589-312	F40161	Fairchild	A-12
589-313	F40194	Fairchild	A-12
589-315	F4013	Fairchild	A-13
589-973	NE5539	Signetics	A-13

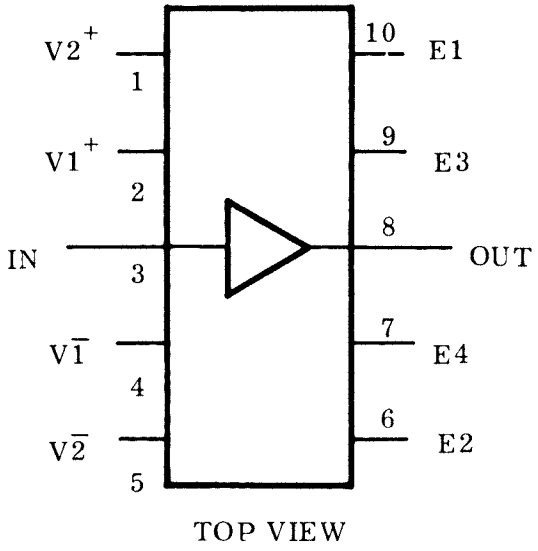
FAIRCHILD	AMPEX	HIGH-SPEED DIFFERENTIAL COMPARATOR
UA710HC	586-124	



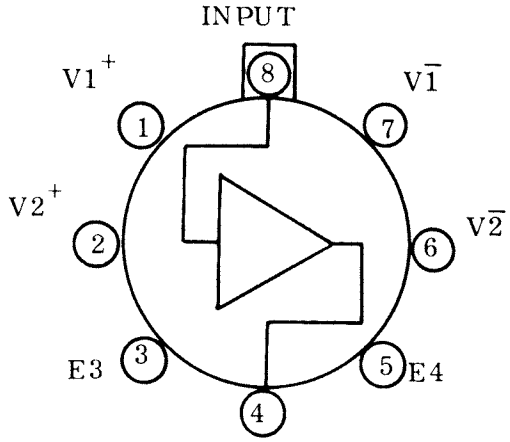


BOTTOM VIEW

NATIONAL SEMI	AMPEX	
LH 0002 C	→ 586-315	CURRENT AMPLIFIER
LH 0002 CN	587-270	



TOP VIEW



OUTPUT
TOP VIEW

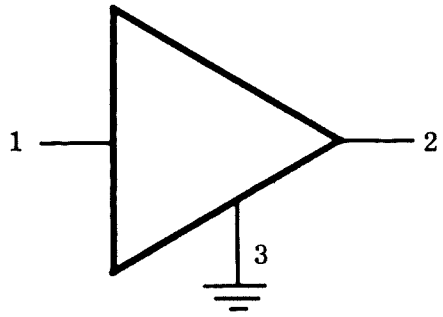
RCA/FAIRCHILD	AMPEX	
F4011PC	587-909	
CD 4011AE	→ 587-319	2 INPUT NAND GATE

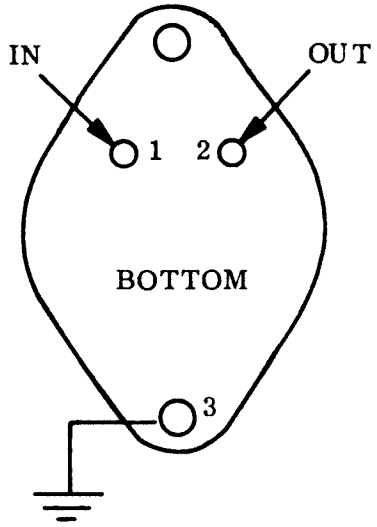
$X = \overline{AB}$

A	B	X
1	2	3
4	5	6
8	9	10
12	13	11

VDD 14
VSS 7

FAIRCHILD	AMPEX	
78L05AWC	587-771	VOLT REG. 5V
7805VC	→ 587-438	

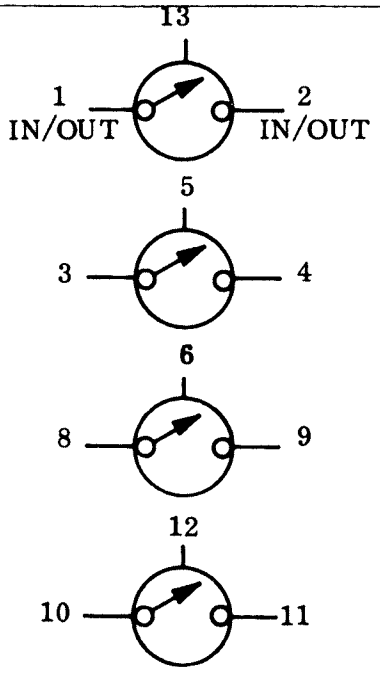




RCA
CD4066

AMPEX
587-680

QUAD BILATERAL SWITCH
C-MOS



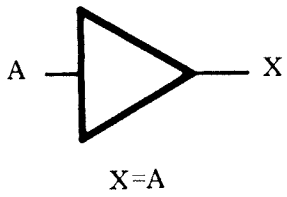
VDD 14
VSS 7

HIGH CLOSES SWITCH

RCA
CD 4010

AMPEX
587-959

HEX CONVERTER



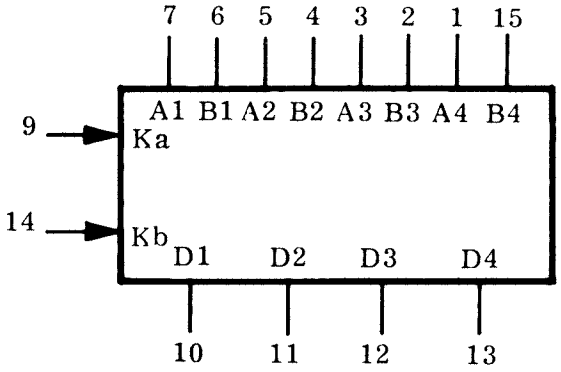
A	X
3	2
5	4
7	6
9	10
11	12
14	15

VCC 1
VDD 16
GND 8

RCA/FAIRCHILD
F4019
CD 4019

AMPEX
587-990
→ 587-960

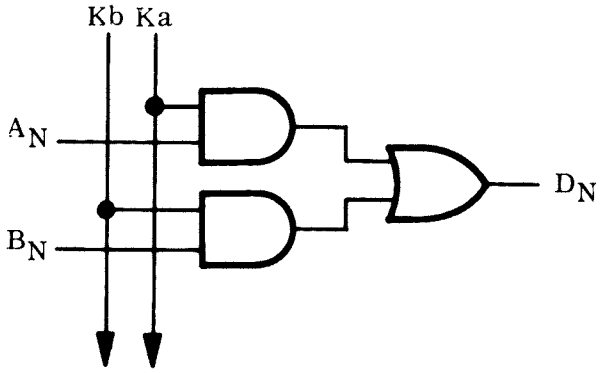
QUAD AND/OR SELECT



VDD 16
VSS 8

LOGIC LIST

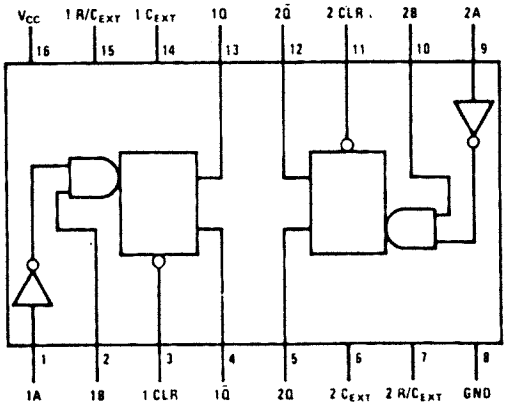
KA	KB	OUTPUT FOLLOWS
H	L	A
L	H	B
L	L	LOW



MOTOROLA
74C221

AMPEX
589-019

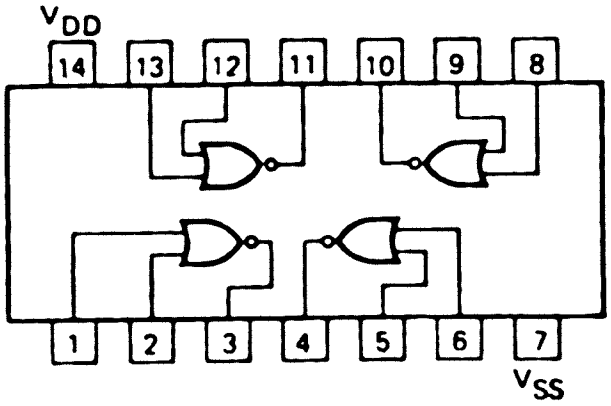
DUAL MONOSTABLE MULTIVIBRATOR



INPUTS			OUTPUTS	
CLEAR	A	B	Q	$\bar{Q}$
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L	↑	⎍	⎴
H	↓	H	⎍	⎴

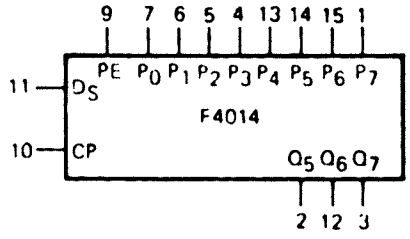
H = High level
L = Low level
↑ = Transition from low to high
↓ = Transition from high to low
⎍ = One high level pulse
⎴ = One low level pulse
X = Irrelevant

FAIRCHILD	AMPEX	QUAD 2-INPUT NOR GATE
F4001	589-298	



Vss = OV Vdd = 5-15V

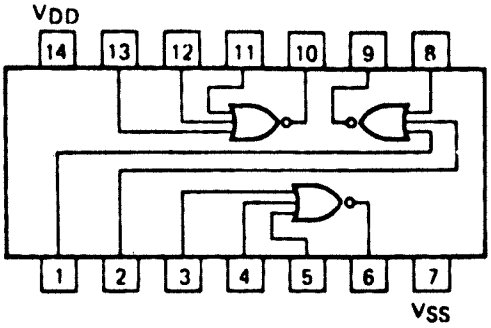
FAIRCHILD	AMPEX	
F4014	589-299	8-BIT SHIFT REGISTER



V_{DD} = Pin 16
V_{SS} = Pin 8

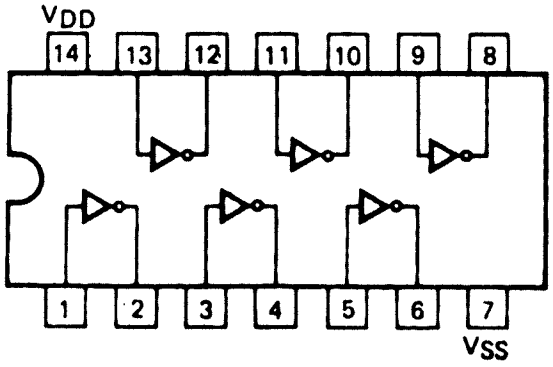
FAIRCHILD	AMPEX	TRIPLE 3-INPUT NOR GATE
F4025	589-300	

LOGIC AND CONNECTION DIAGRAM
DIP (TOP VIEW)



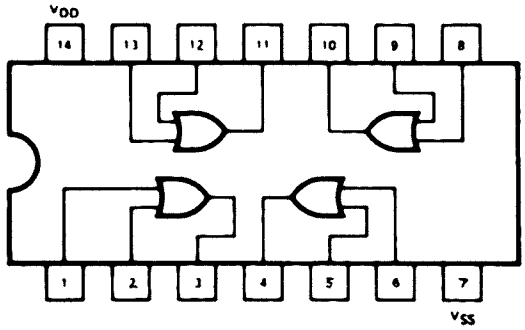
Vss = OV Vdd = 5-15V

FAIRCHILD	AMPEX	HEX INVERTER
F4069	589-301	



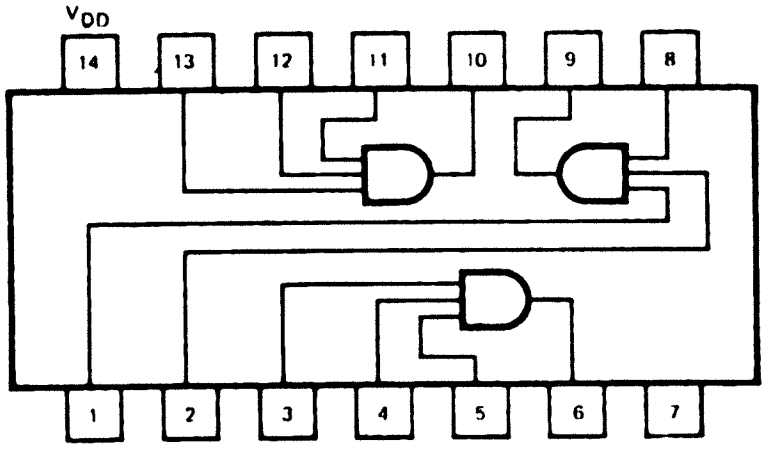
Vss = OV Vdd = 5-15V

FAIRCHILD	AMPEX	
F4071	589-302	QUAD 2-INPUT OR GATE



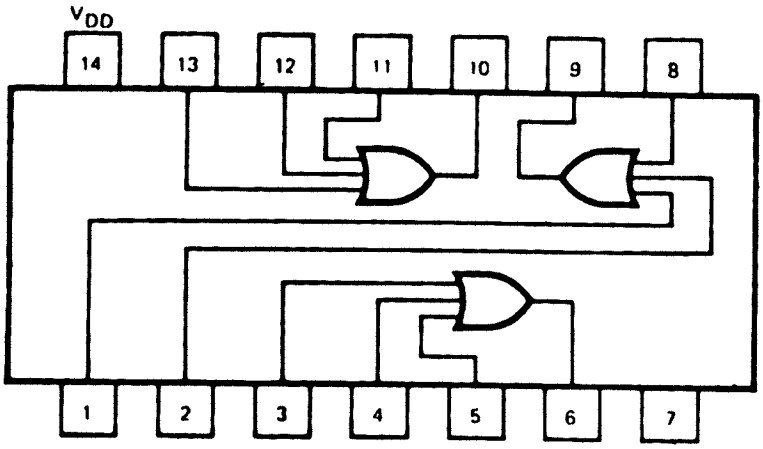
DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V

FAIRCHILD	AMPEX	
F4073	589-303	TRIPLE 3-INPUT AND GATE



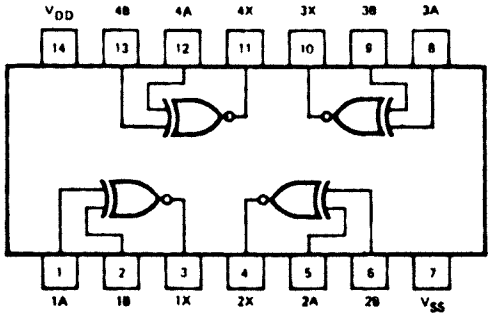
Vss = OV Vdd = 5-15V

FAIRCHILD	AMPEX	TRIPLE 3-INPUT OR GATE
F4075	589-304	



Vss = OV Vdd = 5-15V

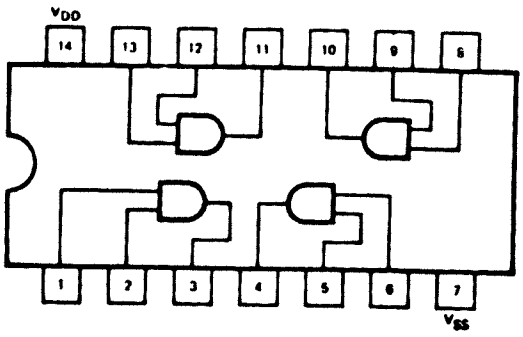
FAIRCHILD	AMPEX	QUAD EXCLUSIVE-NOR GATE
F4077	589-305	



$X = AB + \bar{A}\bar{B}$

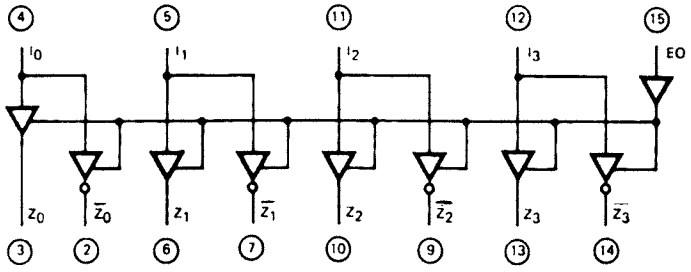
Vss = OV Vdd = 5-15V

FAIRCHILD	AMPEX	QUAD 2-INPUT AND GATE
F4081	589-306	



Vss = OV Vdd = 5-15V

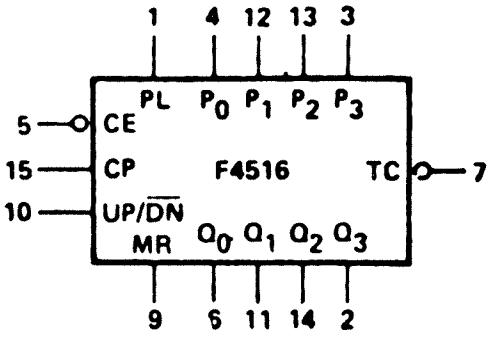
FAIRCHILD	AMPEX	QUAD LOW VOLTAGE TO HIGH VOLTAGE
F4104	589-307	TRANSLATER WITH 3-STATE OUTPUTS



V_{DDO} = Pin 1
V_{DDI} = Pin 16
V_{SS} = Pin 8
O = Pin Number

FAIRCHILD	AMPEX	UP/DOWN COUNTER
F4516	589-308	

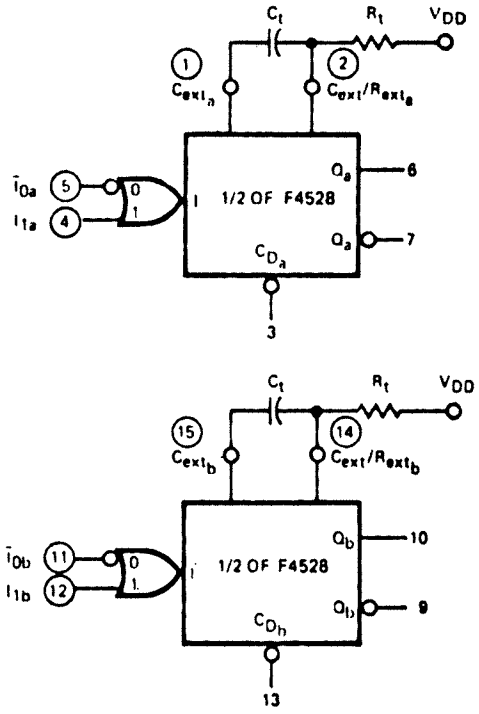
V_{DD} = Pin 16
V_{SS} = Pin 8



PL	UP/$\overline{DN}$	$\overline{CE}$	CP	MODE
H	X	X	X	Parallel Load ($P_n \rightarrow Q_n$)
L	X	H	X	No Change
L	L	L	⌐	Count Down, Binary
L	H	L	⌐	Count Up, Binary

MR = LOW
H = HIGH Level
L = LOW Level
X = Don't Care
⌐ = Positive-Going Transition

FAIRCHILD	AMPEX	DUAL RETRIGGERABLE RESETTABLE
F4528	589-309	MONOSTABLE MULTIVIBRATOR



V_{DD} = Pin 16
V_{SS} = Pin 8

TRUTH TABLE

$\overline{I_0}$	I_1	$\overline{C_D}$	OPERATION
H→L	L	H	Trigger
H	L→H	H	Trigger
X	X	L	Reset

V_{DD} = Pin 16
V_{SS} = Pin 8

FAIRCHILD	AMPEX	64-BIT (16x4) RANDOM ACCESS E MEMORY
F4725	589-310	WITH 3-STATE OUTPUTS

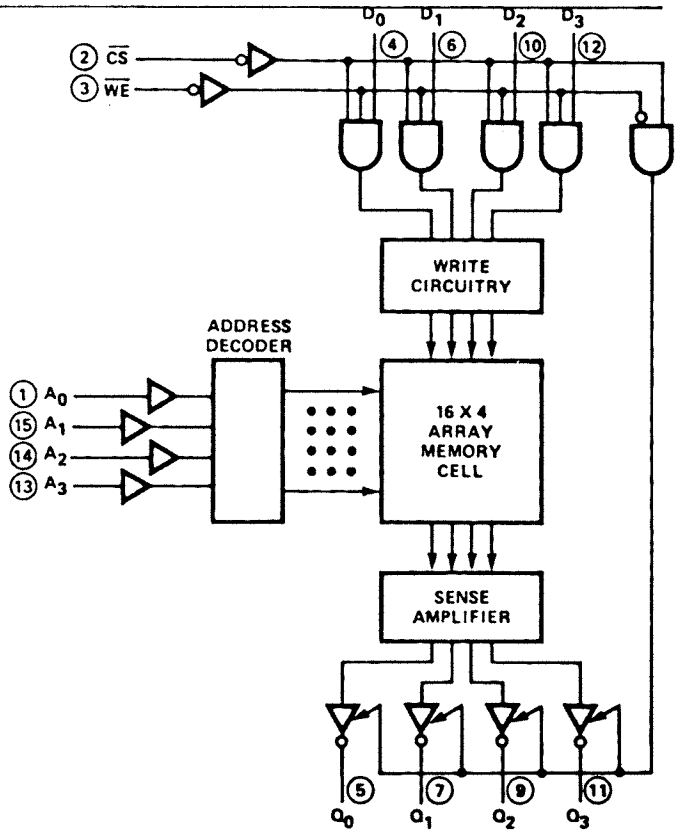
MODE SELECTION

$\overline{CS}$	$\overline{WE}$	OUTPUTS	MODE
L	L	High Impedance	Write
L	H	Outputs are Complement of Data Written into Location	Read
H	X	High Impedance	Inhibit

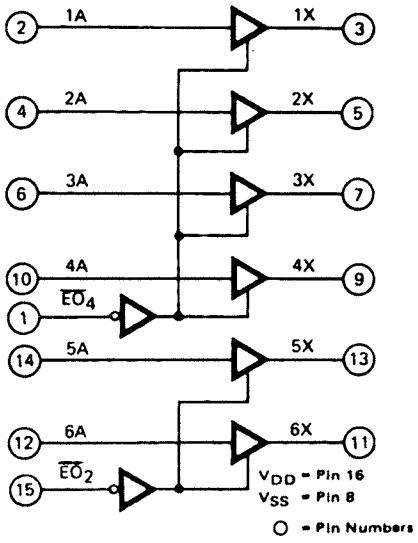
V_{DD}= PIN 16

V_{SS}= PIN 8

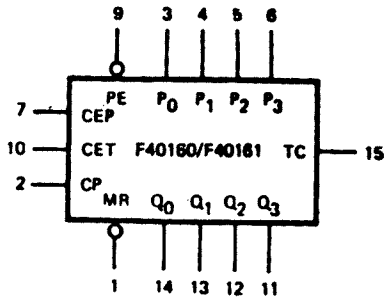
0= PIN NUMBER



FAIRCHILD	AMPEX	3-STATE HEX NON-INVERTING AND
F40097	589-311	INVERTING BUFFERS



FAIRCHILD	AMPEX	4-BIT SYNCHRONOUS COUNTERS
F40161	589-312	



SYNCHRONOUS MODE SELECTION
F40160/F40161

$\overline{PE}$	CEP	CET	MODE
L	X	X	Preset
H	L	X	No Change
H	X	L	No Change
H	H	H	Count

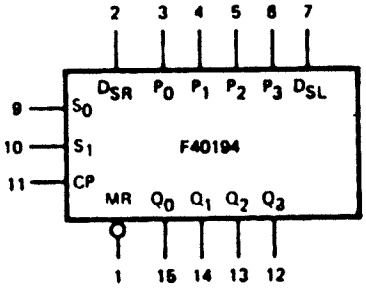
$\overline{MR}$ = HIGH

F40161/F40163 ($Q_0 \cdot Q_1 \cdot Q_2 \cdot Q_3$)	TC
L	L
H	L
L	L
H	H

H = HIGH Level
L = LOW Level
X = Don't Care

$TC = CET \cdot Q_0 \cdot Q_1 \cdot Q_2 \cdot Q_3$ (F40161/F40163)

FAIRCHILD	AMPEX	4-BIT BIDIRECTIONAL UNIVERSAL SHIFT
F40194	589-313	REGISTER



V_{DD} = Pin 16
V_{SS} = Pin 8

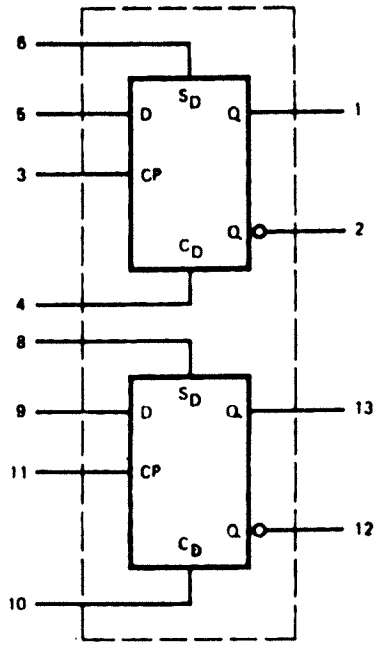
TRUTH TABLE

OPERATING MODE	INPUTS ($\overline{MR}$ = H)					OUTPUTS AT t_{n+1}			
	S_1	S_0	D_{SR}	D_{SL}	P_0,P_1,P_2,P_3	Q_0	Q_1	Q_2	Q_3
Hold	L	L	X	X	X	Q_0	Q_1	Q_2	Q_3
Shift Left	H	L	X	L	X	Q_1	Q_2	Q_3	L
	H	L	X	H	X	Q_1	Q_2	Q_3	H
Shift Right	L	H	L	X	X	L	Q_0	Q_1	Q_2
	L	H	H	X	X	H	Q_0	Q_1	Q_2
Parallel Load	H	H	X	X	L	L	L	L	L
	H	H	X	X	H	H	H	H	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
(t_{n+1}) = Indicates state after next LOW-to-HIGH clock transition.

DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V

FAIRCHILD	AMPEX	DUAL D FLIP FLOP
F4013	589-315	



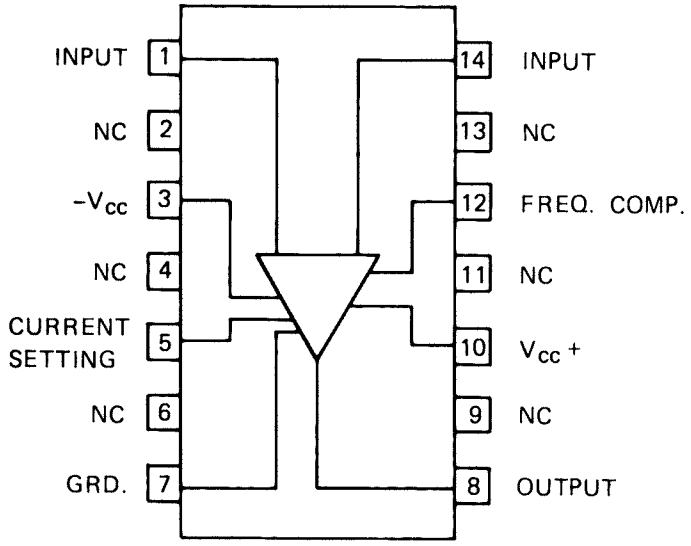
SYNCHRONOUS INPUTS		OUTPUTS	
CP	D	Q_{n+1}	$\overline{Q}_{n+1}$
⌐	L	L	H
⌐	H	H	L

Conditions: $S_D = C_D$ = LOW

ASYNCHRONOUS INPUTS		OUTPUTS	
S_D	C_D	Q	$\overline{Q}$
L	H	L	H
H	L	H	L
H	H	L	L

L = LOW Level
H = HIGH Level
⌐ = Positive-Going Transition
X = Don't Care
Q_{n+1} = State After Clock Positive Transition

SIGNETICS	AMPEX	FAST WIDE BANDWIDTH OPERATIONAL
NE5539	589-973	AMPLIFIER



AMPEX

AUDIO-VIDEO
SYSTEMS DIVISION

CATALOG NO. 1809447-02
CHANGED: JANUARY 1981